

TPS62135EVM-698 Evaluation Module

This user's guide describes the characteristics, operation, and use of TI's TPS62135 evaluation module (EVM). This EVM is designed to help the user easily evaluate and test the operation and functionality of the TPS62135 3.5-A buck converter. The EVM converts a 3-V to 17-V input voltage to a regulated 3.3-V or 5-V output voltage that delivers up to 3.5 A. This user's guide includes setup instructions for the hardware, a printed-circuit board (PCB) layout, a schematic diagram, a bill of materials (BOM), and test results of the EVM.

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1 Introduction

The TPS62135 is a 3.5-A, synchronous, step-down converter in a 3 mm × 2 mm, 11-pin QFN package.

1.1 Performance Specification

Table 1 provides a summary of the TPS62135EVM-698 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification		Test Conditions	MIN	TYP	MAX	Unit
Input voltage			3		17	V
Output voltage setpoint	VSEL = High			5		V
	VSEL = Low			3.3		V
Output current			0		3.5	A
Soft-start time	Ramp time of V_{OUT}			920		μs

1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate the adjustable voltage version of this integrated circuit (IC). On the EVM, additional input and output capacitors can be added, the soft-start time can be changed, the tracking voltage and the input voltage at which the IC turns on can be adjusted. Finally, the loop response of the IC can be measured.

1.2.1 Input and Output Capacitors

C_5 is provided for an additional input capacitor. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple.

C_7 , C_8 , and C_9 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple and to improve the load transient response. For output voltages higher than 5 V, more output capacitance is necessary. The total output capacitance must remain within the recommended range in the TPS62135 data sheet ([SLVSBH3](#)) for proper operation.

1.2.2 Soft-Start Time

C_3 controls the soft-start time of the output voltage on the TPS62135EVM-698. It can be changed for a shorter or slower ramp up of V_{OUT} . Note that as the value of C_3 is decreased, the inrush current increases.

1.2.3 Configurable Tracking Voltage

R_5 and R_6 can be installed to set a user-selectable tracking voltage. See the equations in the data sheet for details of calculating the resistor values.

1.2.4 Configurable Enable Threshold Voltage

With JP_1 removed, R_7 and R_8 can be installed to set a user-selectable input voltage at which the IC turns on. See the equations in the data sheet for details of calculating the resistor values.

1.2.5 Loop Response Measurement

The loop response of the TPS62135EVM-698 can be measured with two simple changes to the circuitry. First, install a 10-Ω resistor across the pads in the middle of the back of the PCB. The pads are spaced to allow installation of 0603-sized resistors. Second, cut the trace between the via on the V_{OS} pin on the top layer and output capacitor. These changes are shown in [Figure 1](#). With these changes, an ac signal (10-mV, peak-to-peak amplitude recommended) can be injected into the control loop across the added resistor.

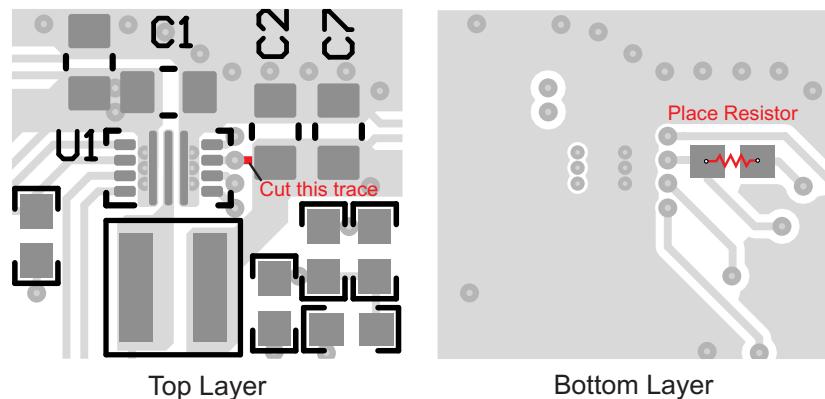


Figure 1. Loop Response Measurement Modification

2 Setup

This section describes how to properly use the TPS62135EVM-698.

2.1 Connector Descriptions

J1, Pin 1 and 2 – VIN	Positive input voltage connection from the input supply for the EVM.
J1, Pin 3 and 4 – S+/S-	Input voltage sense connections. Measure the input voltage at this point.
J1, Pin 5 and 6 – GND	Input return connection from the input supply for the EVM.
J2, Pin 1 and 2 – VOUT	Positive output voltage connection.
J2, Pin 3 and 4 – S+/S-	Output voltage sense connections. Measure the output voltage at this point.
J2, Pin 5 and 6 – GND	Output return connection.
J3 – SS/TR/GND	The SS/TR pin voltage appears on pin 1 of this header with a convenient ground on pin 3.
J3 – TRACK-IN	The TRACK-IN pin can be used to scale down a tracking-voltage.
J4 – PG/GND	The PG output appears on pin 1 of this header with a convenient ground on pin 2.
JP1 – EN	EN pin jumper. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.
JP2 – MODE	Mode pin jumper. Place the supplied jumper across PWM and MODE to operate the converter in a forced PWM mode. Place the jumper across MODE and PFM to operate the converter in power-saving mode.
JP3 – VSEL	VSEL pin jumper. Place the supplied jumper across LOW and VSEL for 3.3-V output. Place the jumper across HIGH and VSEL for 5-V output.
JP4 – PG Pullup Voltage	PG pin pullup voltage jumper. Place the supplied jumper on JP4 to connect the PG pin pullup resistor to the output voltage. Alternatively, the jumper can be removed and a different voltage can be supplied on pin 1 to pull up the PG pin to a different level. This externally applied voltage must remain below 6 V.

2.2 Setup

To operate the EVM, set jumpers JP1 through JP4 to the desired positions per [Section 2.1](#). Connect the input supply to J1, and connect the load to J2.

3 TPS62135EVM-698 Test Results

This section provides test results of the TPS62135EVM-698.

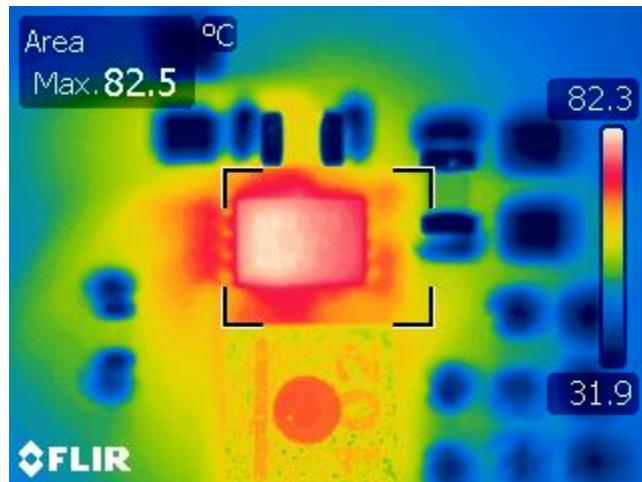


Figure 2. Thermal Performance ($V_{IN} = 12$ V, $V_{OUT} = 3.3$ V, Load = 3.5 A, Mode = Low)

4 Board Layout

This section provides the TPS62135EVM-698 board layout and illustrations. The Gerbers are available on the EVM product page: TPS62135EVM-698.

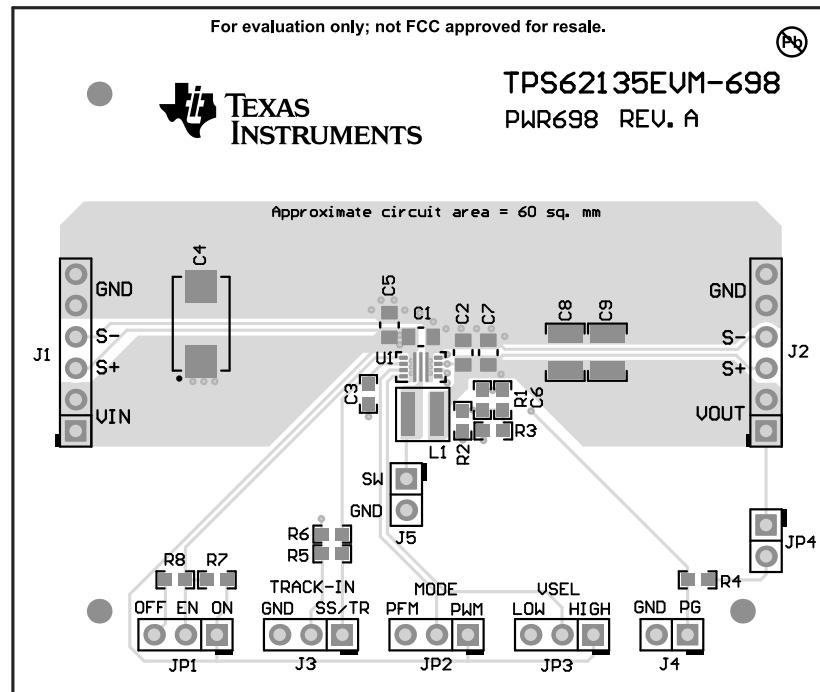


Figure 3. Top Assembly

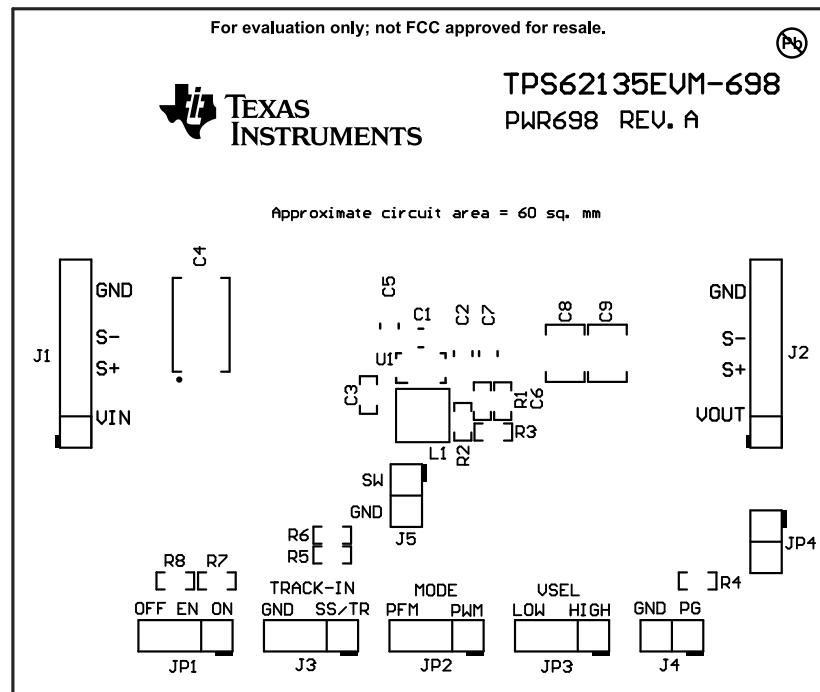


Figure 4. Top Overlay

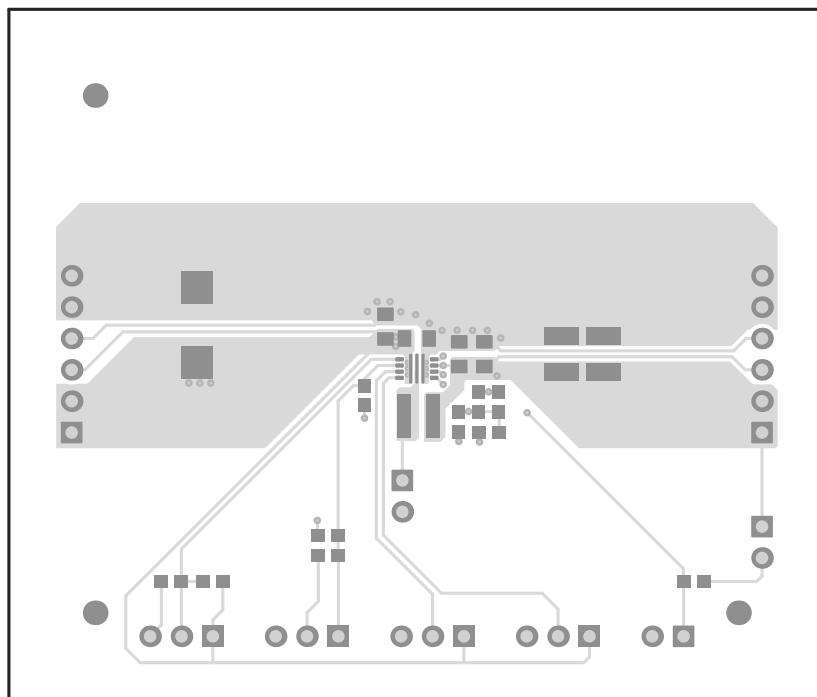


Figure 5. Top Layer

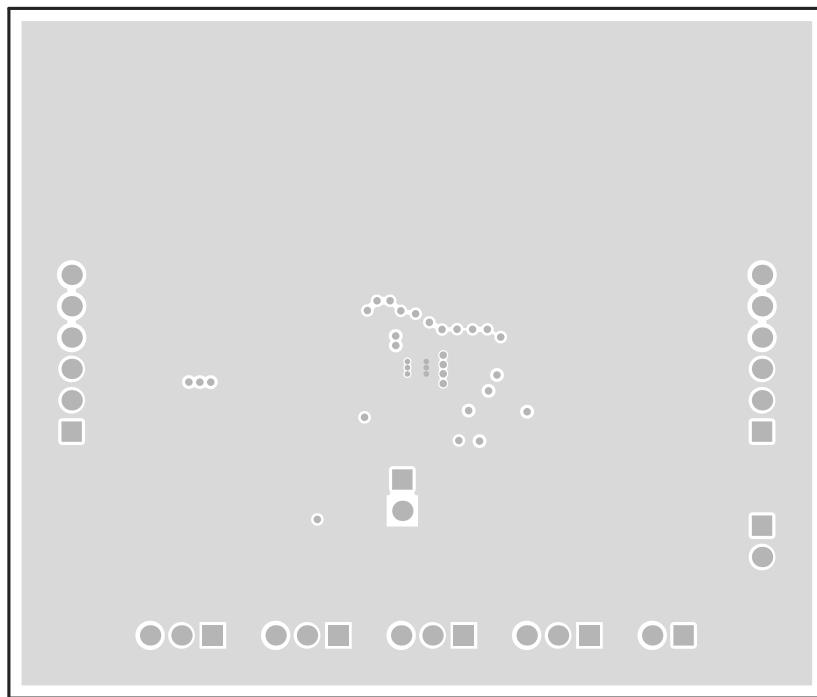


Figure 6. Internal Layer 1

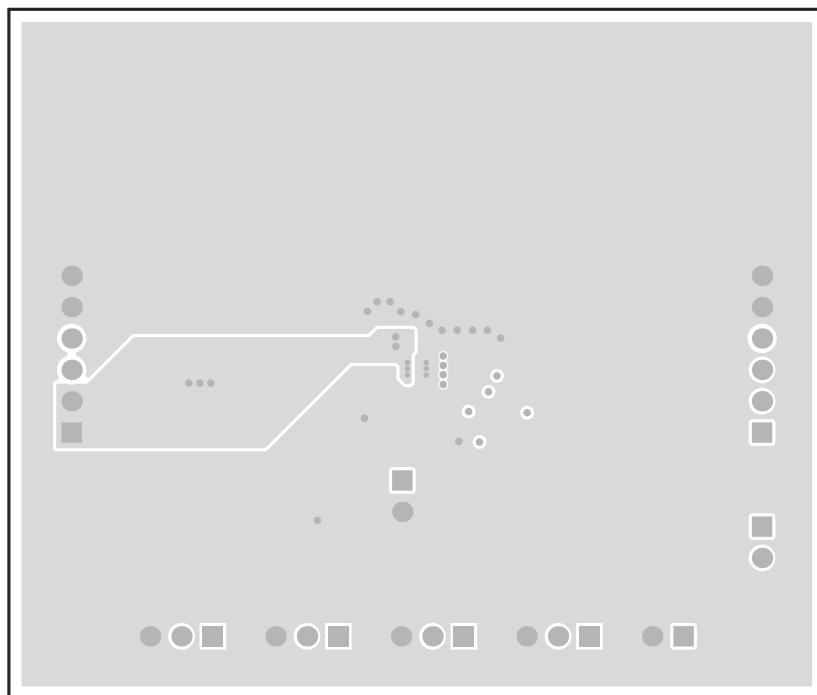


Figure 7. Internal Layer 2

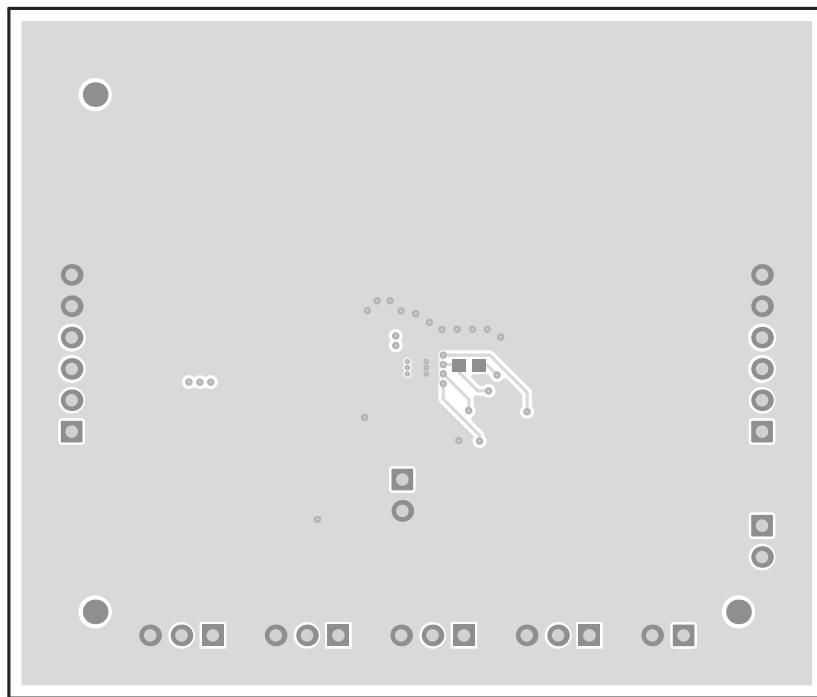


Figure 8. Bottom Layer

5 Schematic and Bill of Materials

This section provides the TPS62135EVM-698 schematic and bill of materials.

5.1 Schematic

Figure 9 illustrates the EVM schematic.

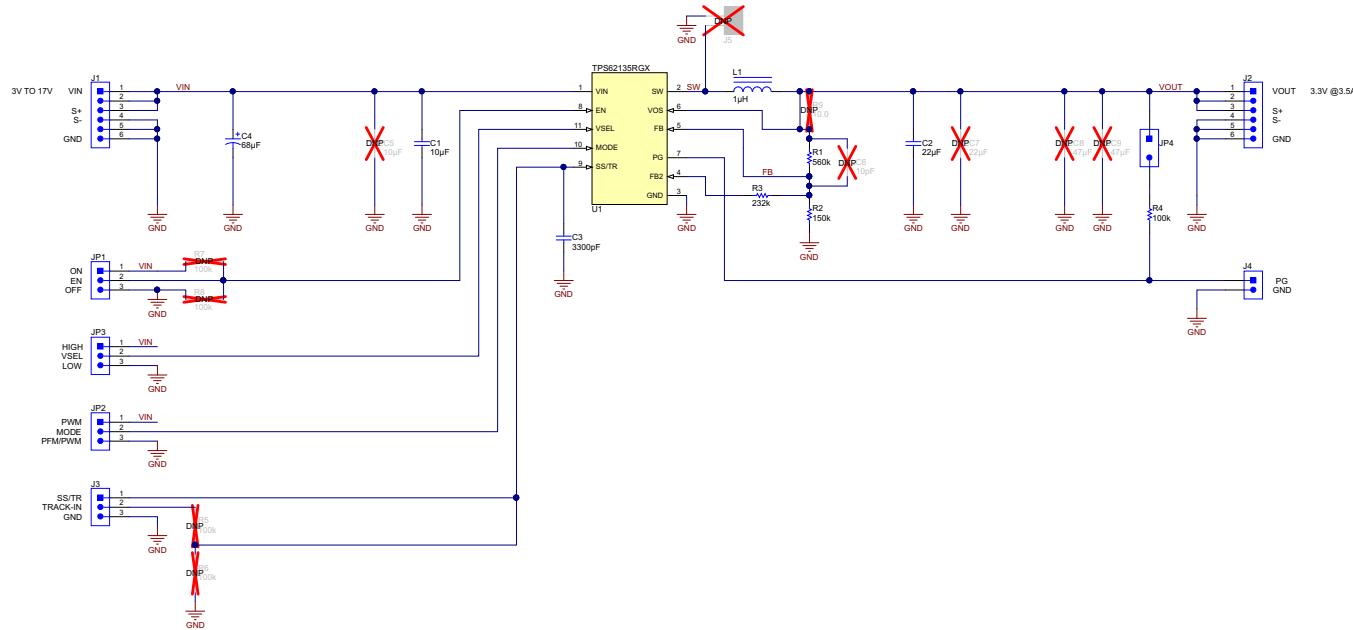


Figure 9. TPS62135EVM-698 Schematic

5.2 Bill of Materials

Table 2 lists the BOM for this EVM.

Table 2. TPS62135EVM-698 Bill of Materials

Qty	Ref Des	Value	Description	Size	Part Number	Manufacturer
1	C1	10 μ F	Capacitor, Ceramic, 25V, X5R, $\pm 10\%$	0805	TMK212BBJ106KG-T	Taiyo Yuden
1	C2	22 μ F	Capacitor, Ceramic, 16V, X5R, $\pm 20\%$	0805	EMK212BBJ226MG-T	Taiyo Yuden
1	C3	3300 pF	Capacitor, Ceramic, 50V, C0G/NP0, $\pm 5\%$	0603	Std	Std
1	C4	68 μ F	Capacitor, Tantalum, 35V, 68uF, $\pm 20\%$	7343-43	TPSE686M025R0125	AVX
1	L1	1.0 μ H	Inductor, Shielded, 5.4A, 0.01 ohm, $\pm 20\%$	4x4x2mm	XFL4020-102MEB	Coilcraft
1	R1	560k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	150k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	232k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS62135	IC, 17V 3.5A Step-Down Converter	2 x 3 mm	TPS62135RGX	Texas Instruments

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

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Concernant les EVMs avec antennes détachables

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