

## Automotive N-Channel 40 V (D-S) 175 °C MOSFET

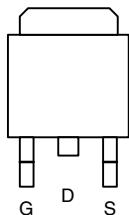
PRODUCT SUMMARY	
$V_{DS}$ (V)	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0041
$I_D$ (A)	50
Configuration	Single

### FEATURES

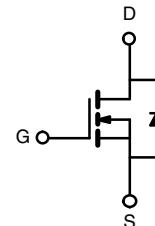
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified<sup>d</sup>
- 100 %  $R_g$  and UIS Tested
- Material categorization:  
For definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



TO-263



Top View



N-Channel MOSFET

### ORDERING INFORMATION

Package	TO-263
Lead (Pb)-free and Halogen-free	SQM50N04-4m1-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$I_D$	50	A
		50	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	50	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	200	
Single Pulse Avalanche Current	$I_{AS}$	60	mJ
Single Pulse Avalanche Energy	$E_{AS}$	180	
Maximum Power Dissipation <sup>b</sup>	$P_D$	150	W
		50	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	1	

#### Notes

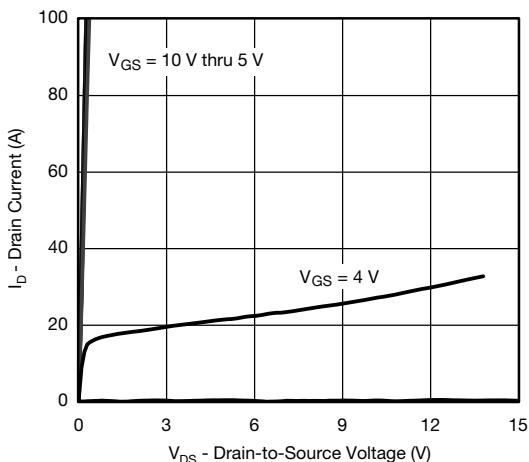
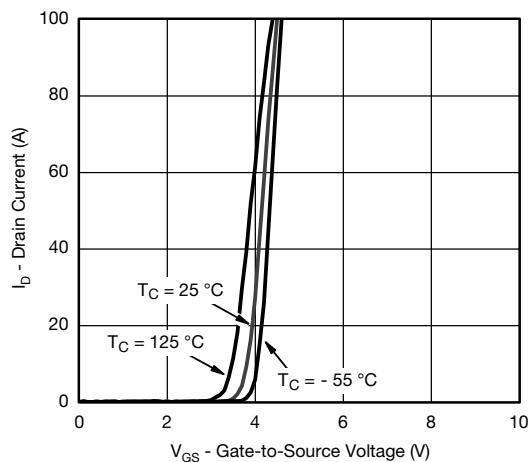
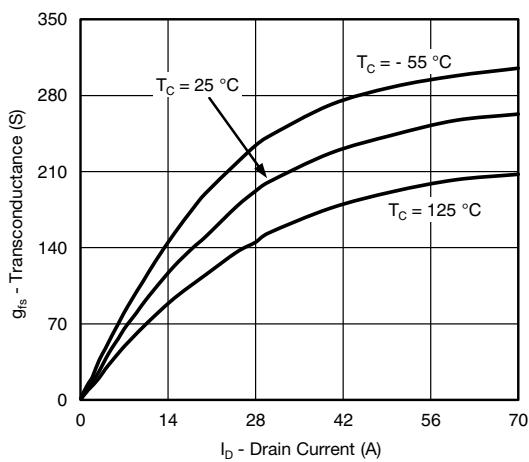
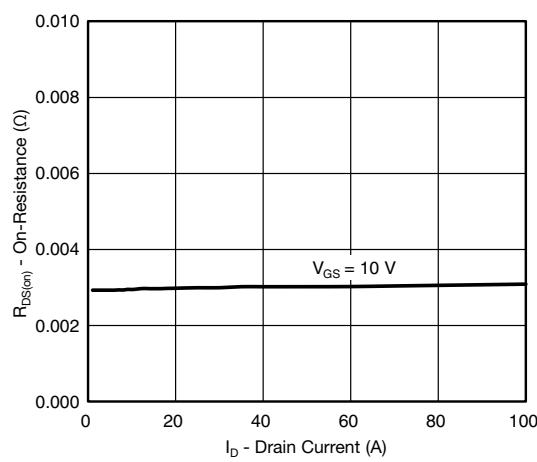
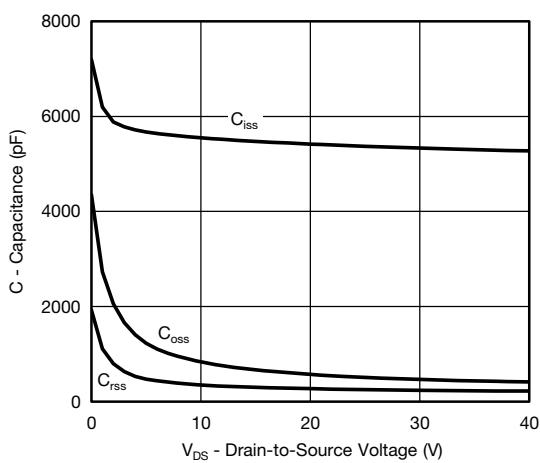
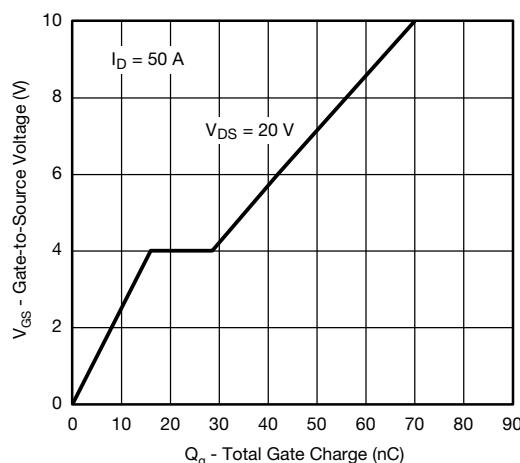
- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

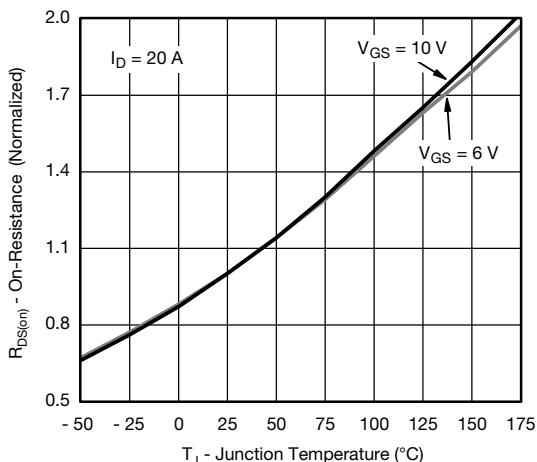
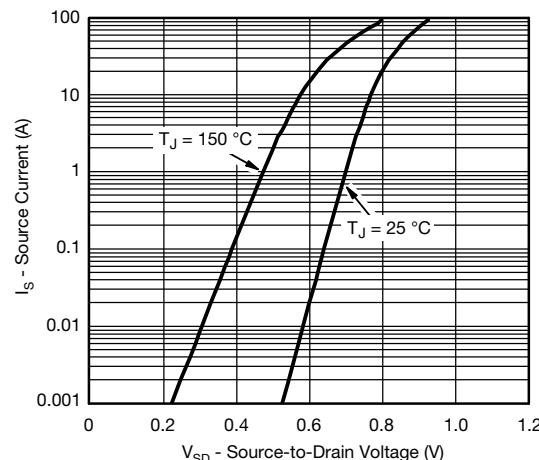
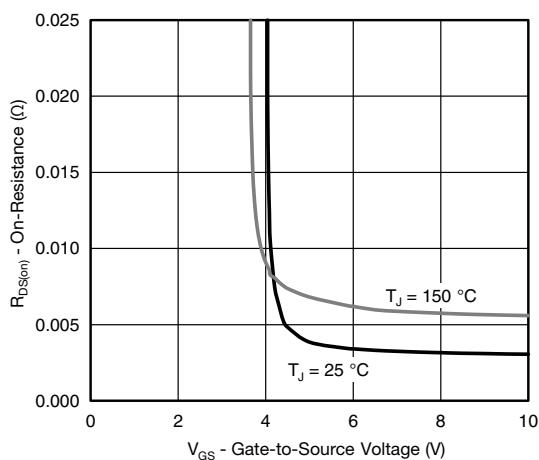
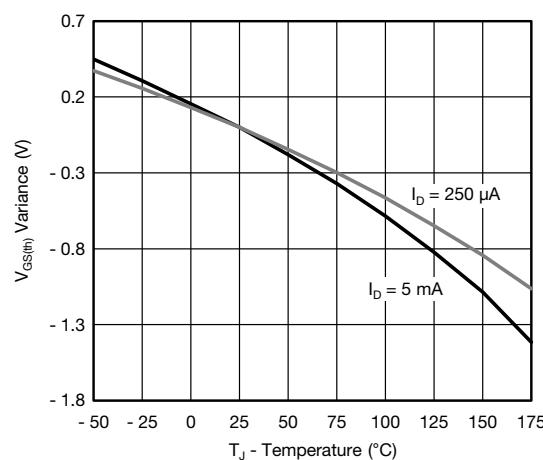
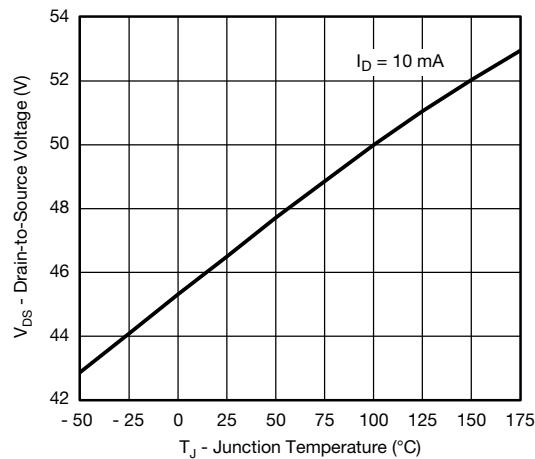
<b>SPECIFICATIONS</b> ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		40	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.5	3.0	3.5		
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	$\mu\text{A}$	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$ , $T_J = 125^\circ\text{C}$	-	-	50		
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$ , $T_J = 175^\circ\text{C}$	-	-	250		
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	50	-	-	A	
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$	-	0.0030	0.0041	$\Omega$	
		$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$ , $T_J = 125^\circ\text{C}$	-	-	0.0068		
		$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$ , $T_J = 175^\circ\text{C}$	-	-	0.0082		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 30\text{ A}$		-	200	-	S	
<b>Dynamic<sup>b</sup></b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$	-	5372	6715	pF	
Output Capacitance	$C_{oss}$			-	512	640		
Reverse Transfer Capacitance	$C_{rss}$			-	256	320		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}$ , $I_D = 50\text{ A}$	-	70	105	nC	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	16	-		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	12.6	-		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		0.9	1.86	2.8	$\Omega$	
Turn-On Delay Time <sup>c</sup>	$t_{d(\text{on})}$	$V_{DD} = 20\text{ V}$ , $R_L = 0.4\text{ }\Omega$ $I_D \geq 50\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$		-	12	18	ns	
Rise Time <sup>c</sup>	$t_r$			-	5	8		
Turn-Off Delay Time <sup>c</sup>	$t_{d(\text{off})}$			-	35	53		
Fall Time <sup>c</sup>	$t_f$			-	9	14		
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>								
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	200	A	
Forward Voltage	$V_{SD}$	$I_F = 50\text{ A}$ , $V_{GS} = 0\text{ V}$		-	0.86	1.5	V	

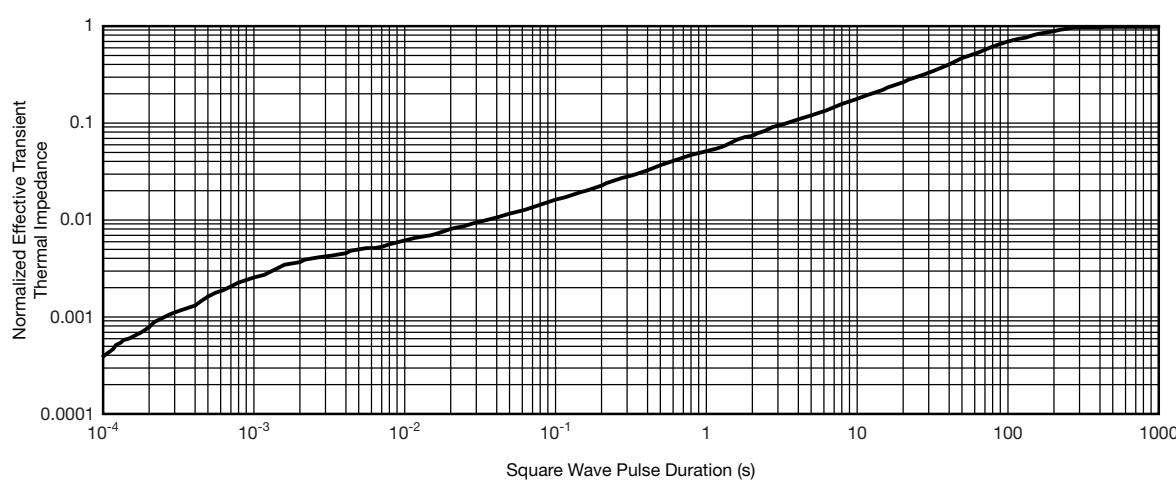
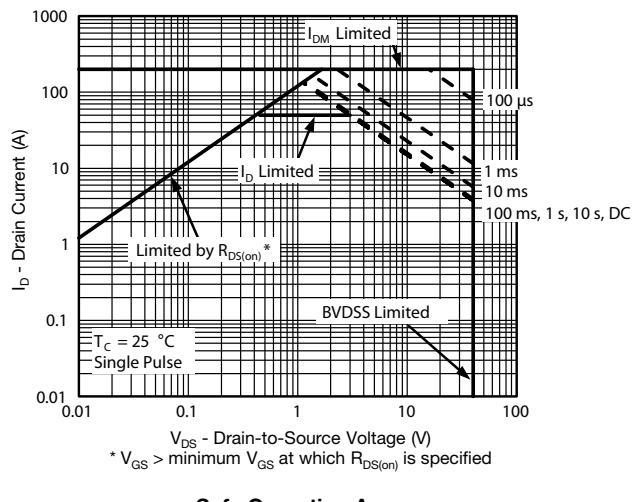
**Notes**

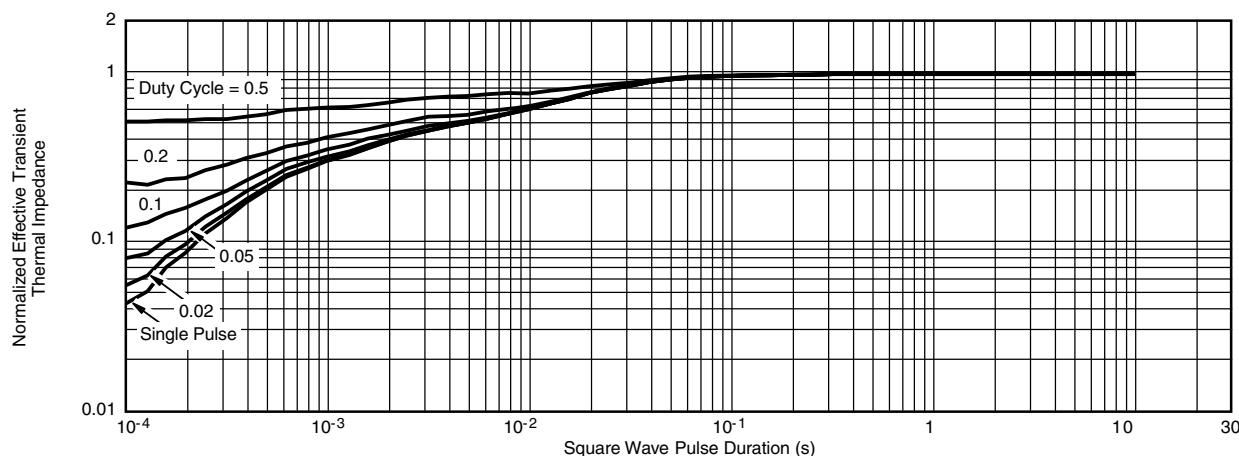
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\text{ \%}$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**On-Resistance vs. Junction Temperature**

**Source Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Drain Source Breakdown vs. Junction Temperature**

**THERMAL RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)**


**THERMAL RATINGS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Case**
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63770](http://www.vishay.com/ppg?63770).

## D<sup>2</sup>PAK / TO-263 and TO-262

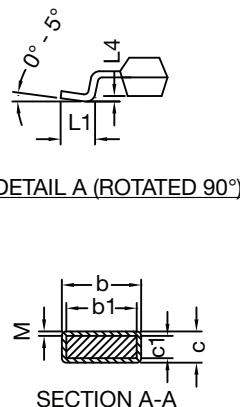
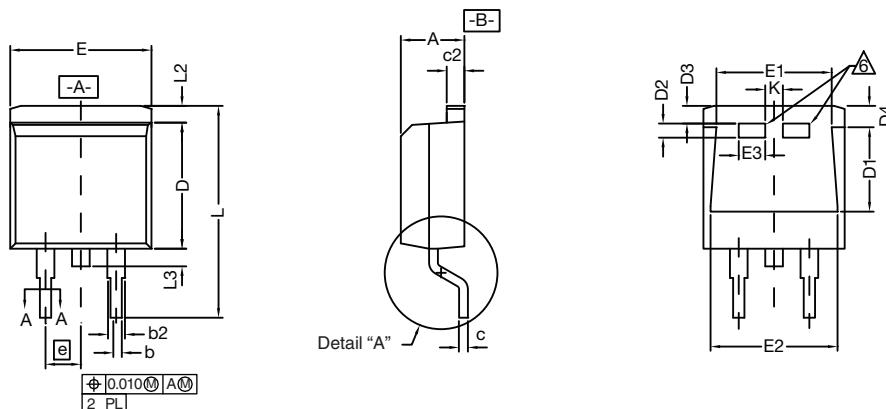
Ordering codes for the SQ rugged series power MOSFETs in the D<sup>2</sup>PAK / TO-263 and TO-262 packages:

DATASHEET PART NUMBER	OLD ORDERING CODE <sup>a</sup>	NEW ORDERING CODE
SQM100N04-2m7	SQM100N04-2M7-GE3	<b>SQM100N04-2M7_GE3</b>
SQM100N10-10	SQM100N10-10-GE3	<b>SQM100N10-10_GE3</b>
SQM110N05-06L	SQM110N05-06L-GE3	<b>SQM110N05-06L_GE3</b>
SQM110P06-8m9L	SQM110P06-8M9L-GE3	<b>SQM110P06-8M9L_GE3</b>
SQM120N02-1m3L	SQM120N02-1M3L-GE3	<b>SQM120N02-1M3L_GE3</b>
SQM120N03-1m5L	SQM120N03-1M5L-GE3	<b>SQM120N03-1M5L_GE3</b>
SQM120N04-1m7	SQM120N04-1M7-GE3	<b>SQM120N04-1M7_GE3</b>
SQM120N04-1m7L	SQM120N04-1M7L-GE3	<b>SQM120N04-1M7L_GE3</b>
SQM120N04-1m9	SQM120N04-1M9-GE3	<b>SQM120N04-1M9_GE3</b>
SQM120N06-06	SQM120N06-06-GE3	<b>SQM120N06-06_GE3</b>
SQM120N06-3m5L	SQM120N06-3M5L-GE3	<b>SQM120N06-3M5L_GE3</b>
SQM120N10-09	SQM120N10-09-GE3	<b>SQM120N10-09_GE3</b>
SQM120N10-3m8	SQM120N10-3M8-GE3	<b>SQM120N10-3M8_GE3</b>
SQM120P04-04L	SQM120P04-04L-GE3	<b>SQM120P04-04L_GE3</b>
SQM120P06-07L	SQM120P06-07L-GE3	<b>SQM120P06-07L_GE3</b>
SQM200N04-1m1L	SQM200N04-1M1L-GE3	<b>SQM200N04-1M1L_GE3</b>
SQM200N04-1m7L	SQM200N04-1M7L-GE3	<b>SQM200N04-1M7L_GE3</b>
SQM200N04-1m8	SQM200N04-1M8-GE3	<b>SQM200N04-1M8_GE3</b>
SQM25N15-52	SQM25N15-52-GE3	<b>SQM25N15-52_GE3</b>
SQM35N30-97	SQM35N30-97-GE3	<b>SQM35N30-97_GE3</b>
SQM40N10-30	SQM40N10-30-GE3	<b>SQM40N10-30_GE3</b>
SQM40N15-38	SQM40N15-38-GE3	<b>SQM40N15-38_GE3</b>
SQM40P10-40L	SQM40P10-40L-GE3	<b>SQM40P10-40L_GE3</b>
SQM47N10-24L	SQM47N10-24L-GE3	<b>SQM47N10-24L_GE3</b>
SQM50020EL	-	<b>SQM50020EL_GE3</b>
SQM50N04-4m0L	SQM50N04-4M0L-GE3	<b>SQM50N04-4M0L_GE3</b>
SQM50N04-4m1	SQM50N04-4M1-GE3	<b>SQM50N04-4M1_GE3</b>
SQM50P03-07	SQM50P03-07-GE3	<b>SQM50P03-07_GE3</b>
SQM50P04-09L	SQM50P04-09L-GE3	<b>SQM50P04-09L_GE3</b>
SQM50P06-15L	SQM50P06-15L-GE3	<b>SQM50P06-15L_GE3</b>
SQM50P08-25L	SQM50P08-25L-GE3	<b>SQM50P08-25L_GE3</b>
SQM60N06-15	SQM60N06-15-GE3	<b>SQM60N06-15_GE3</b>
SQM60N20-35	SQM60N20-35-GE3	<b>SQM60N20-35_GE3</b>
SQM85N15-19	SQM85N15-19-GE3	<b>SQM85N15-19_GE3</b>
SQV120N10-3m8	SQV120N10-3m8-GE3	<b>SQV120N10-3m8_GE3</b>
SQV120N06-4m7L	-	<b>SQV120N06-4m7L_GE3</b>

**Note**

a. Old ordering code is obsolete and no longer valid for new orders

### TO-263 (D<sup>2</sup>PAK): 3-LEAD

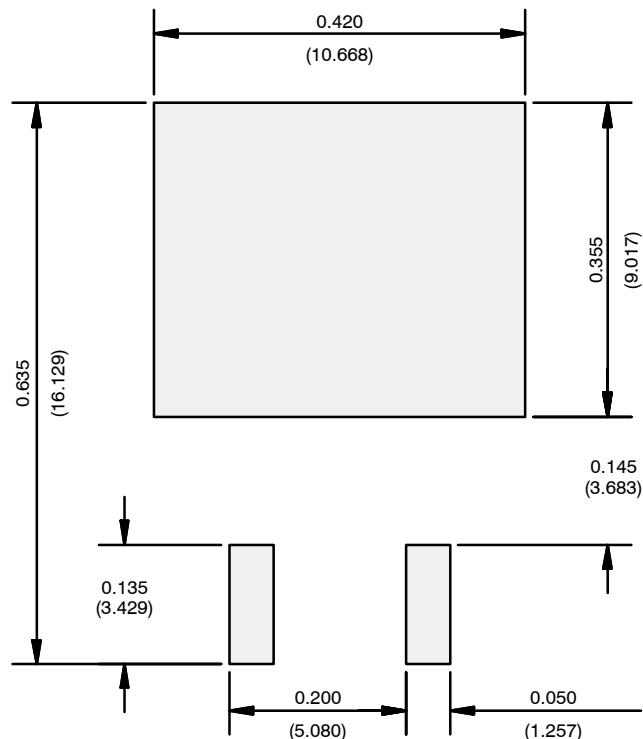


#### Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.

 This feature is for thick lead.

DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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