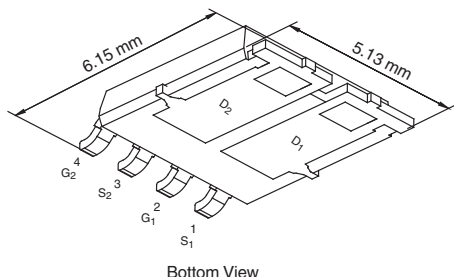


Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.014
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.015
I_D (A) per leg	8
Configuration	Dual

PowerPAK® SO-8L Dual



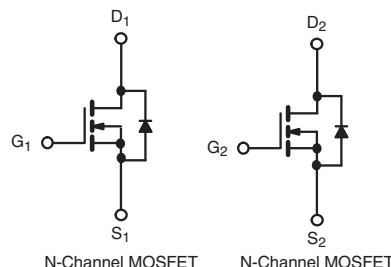
Bottom View

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC
- AEC-Q101 Qualified^d



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

N-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ912EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	8	A
		8	
Continuous Source Current (Diode Conduction) ^a	I_S	8	
Pulsed Drain Current ^b	I_{DM}	32	
Single Pulse Avalanche Current	I_{AS}	33	mJ
Single Pulse Avalanche Energy	E_{AS}	56	
Maximum Power Dissipation ^b	P_D	48	W
		16	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	85	°C/W
Junction-to-Case (Drain)	R_{thJC}	3.1	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection..
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

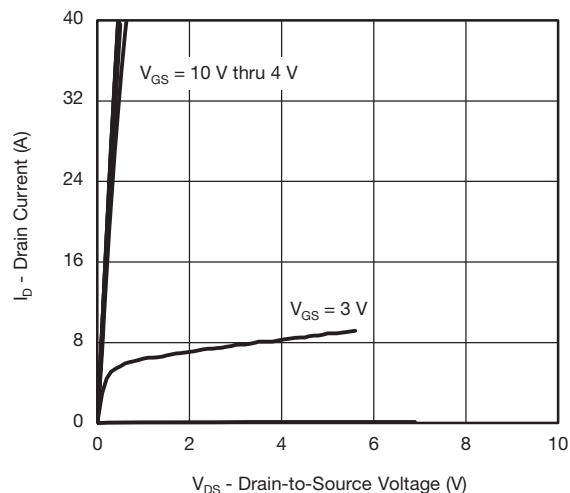
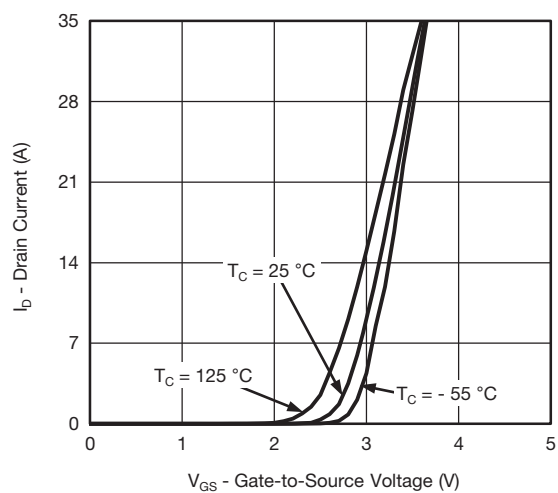
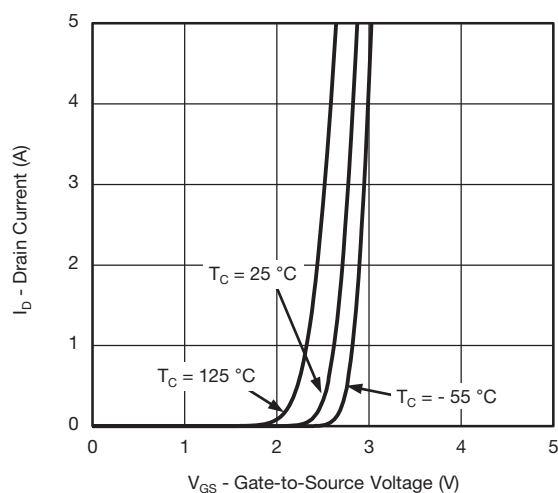
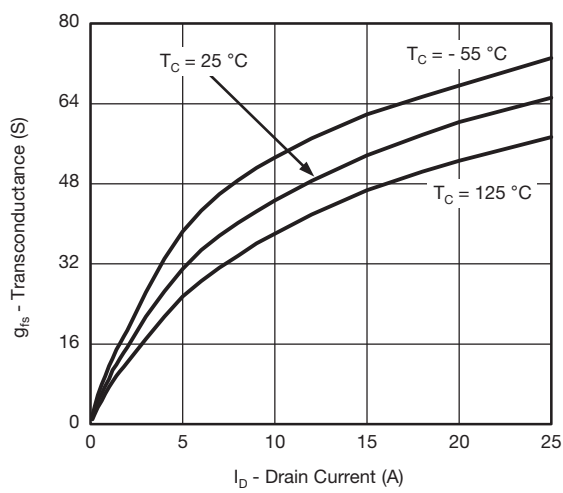
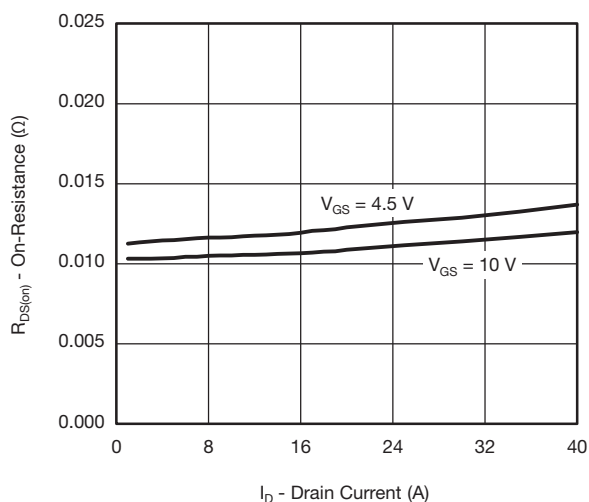
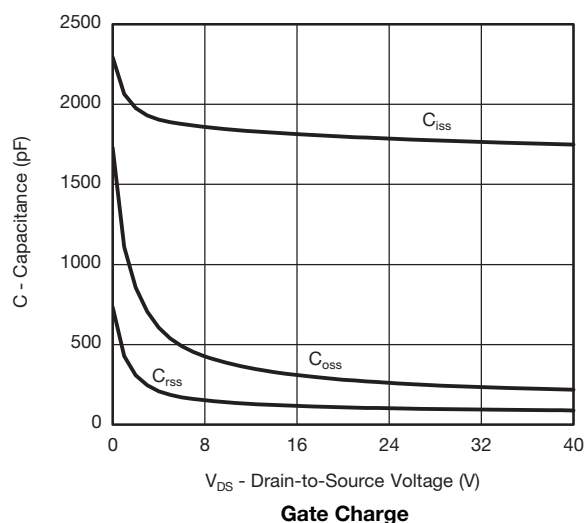


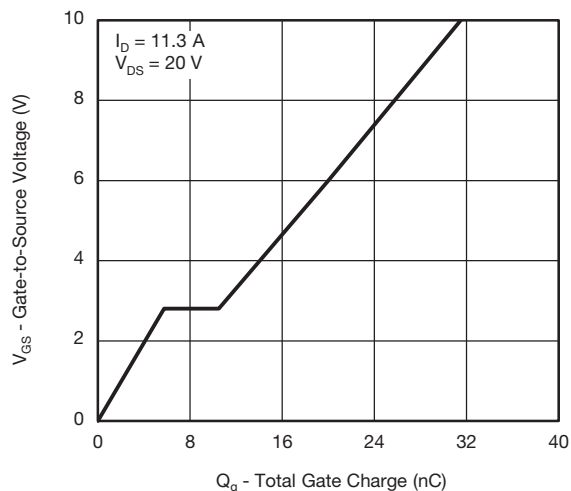
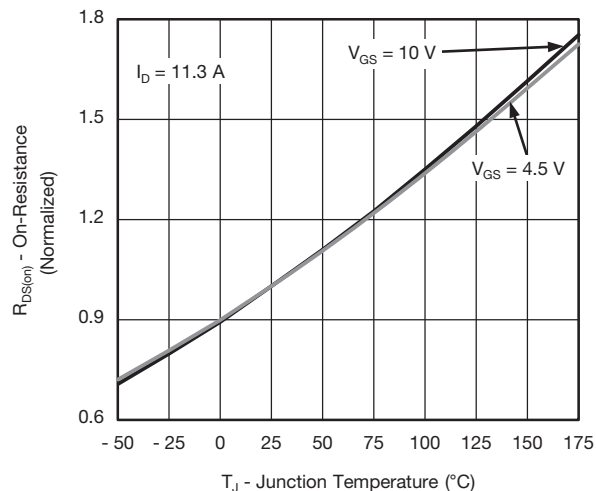
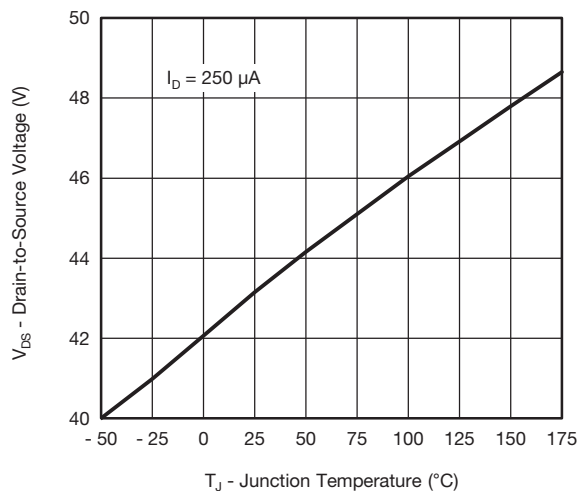
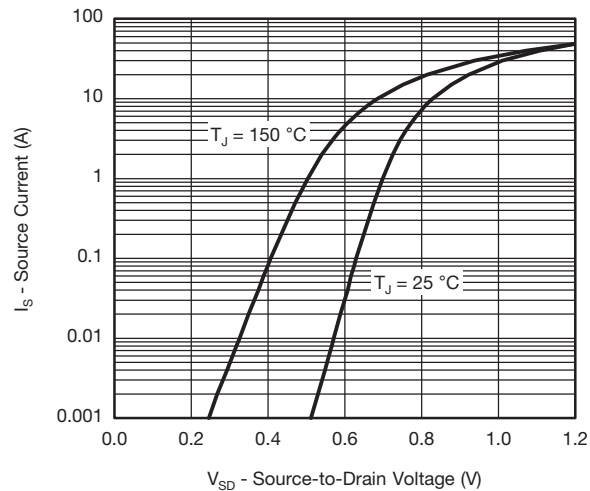
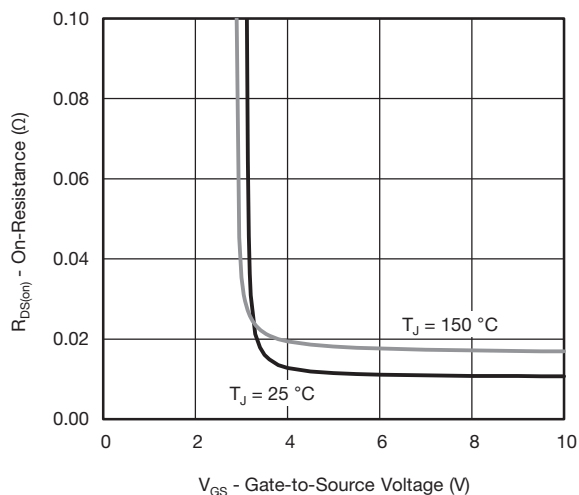
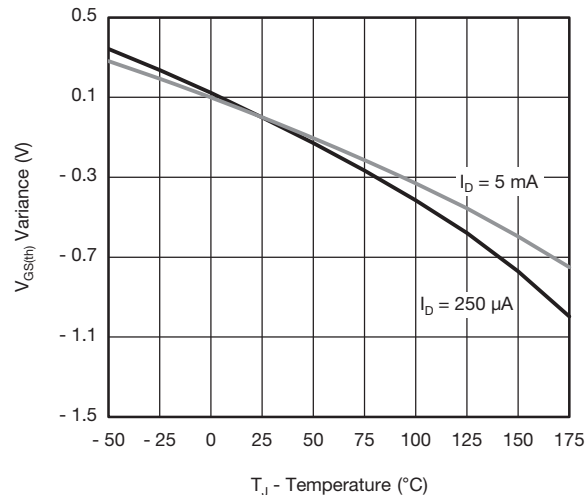
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		40	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.3	1.8	2.3	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 11 A	-	0.011	0.014	Ω
		V _{GS} = 4.5 V	I _D = 8 A	-	0.012	0.015	
		V _{GS} = 10 V	I _D = 11 A, T _J = 125 °C	-	-	0.021	
		V _{GS} = 10 V	I _D = 11 A, T _J = 175 °C	-	-	0.025	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 10 A		-	44	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	-	1799	2248	pF
Output Capacitance	C _{oss}			-	282	352	
Reverse Transfer Capacitance	C _{rss}			-	109	136	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 11.3 A	-	31.5	48	nC
Gate-Source Charge ^c	Q _{gs}			-	5.7	-	
Gate-Drain Charge ^c	Q _{gd}			-	4.8	-	
Gate Resistance	R _g	f = 1 MHz		2.1	4.3	7	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 1.77 Ω I _D ≅ 11.3 A, V _{GEN} = 10 V, R _g = 1 Ω		-	7	11	ns
Rise Time ^c	t _r			-	21	32	
Turn-Off Delay Time ^c	t _{d(off)}			-	33	50	
Fall Time ^c	t _f			-	19	29	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	32	A
Forward Voltage	V _{SD}	I _F = 8 A, V _{GS} = 0 V		-	0.8	1.1	V

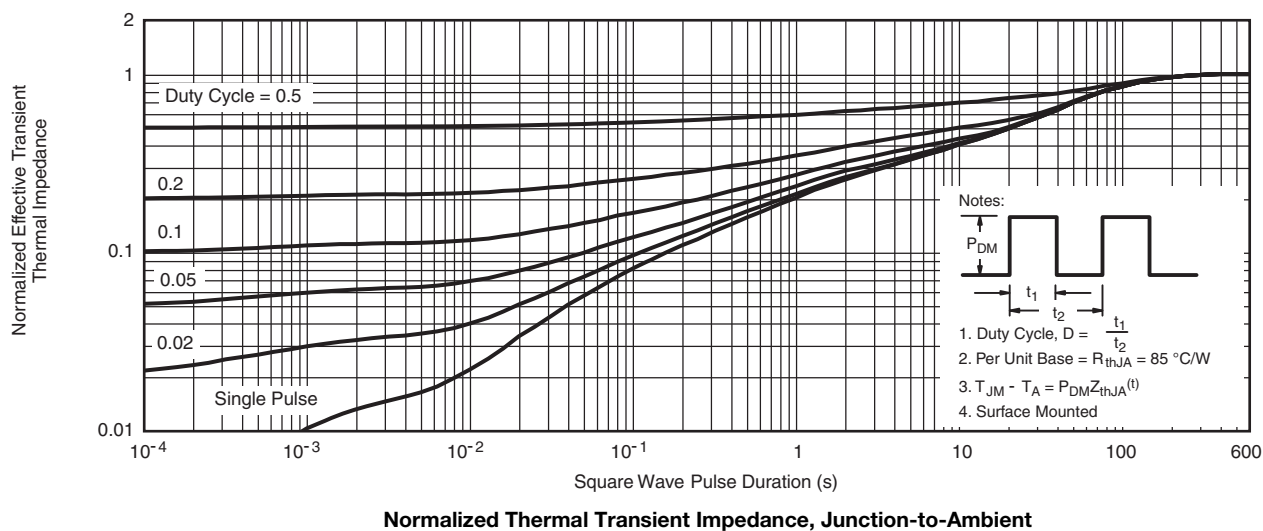
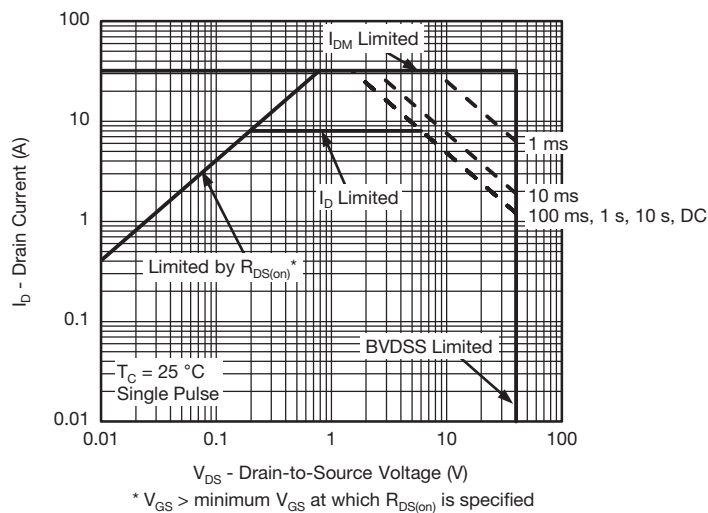
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

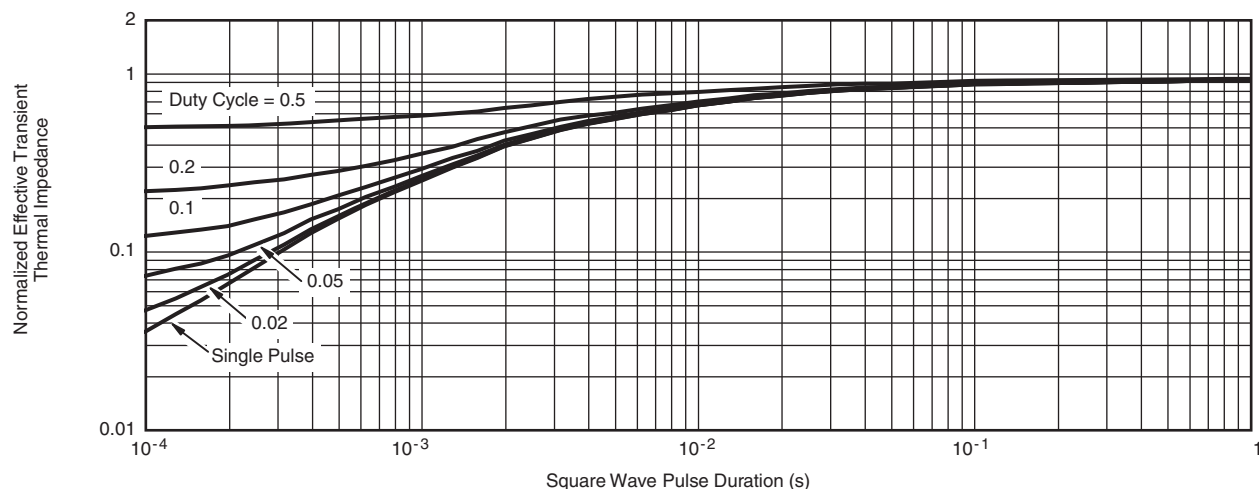
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

Capacitance

Gate Charge

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Drain Current

Drain-Source Breakdown vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

On-Resistance vs. Junction Temperature

Threshold Voltage

THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)




THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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