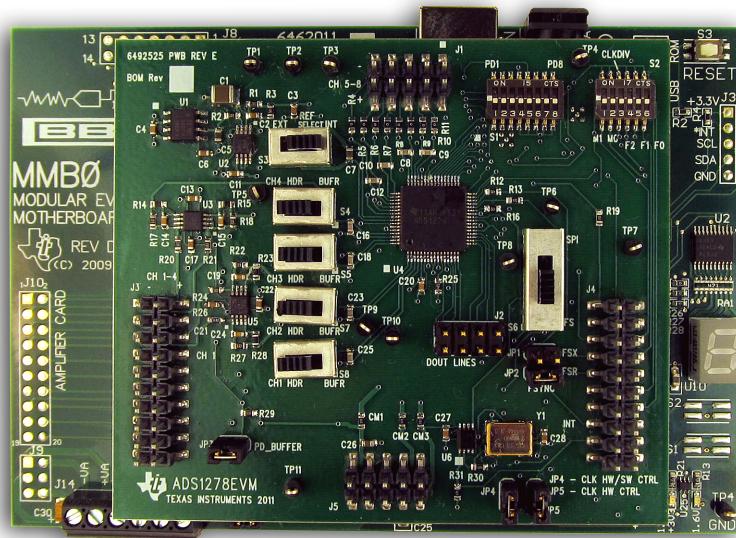


ADS1x7xEVM-PDK



ADS1x7xEVM-PDK

This user's guide describes the characteristics, operation, and use of the ADS1x7xEVM-PDK. These evaluation modules kits (EVM-PDK) are an evaluation system for the [ADS1278](#), a 24-bit, 8 channel, delta-sigma analog-to-digital converter (ADC), the [ADS1178](#), a 16-bit version of the ADS1278 and the [ADS1274](#) and [ADS1174](#), which are 4 channel versions of the ADS1278 and ADS1178, respectively. The EVM-PDK allows evaluation of all aspects of the ADS1x7x devices.

This document includes an EVM QuickStart, hardware and software details, bill of materials, and schematic.

The following related documents are available through the Texas Instruments web site at <http://www.ti.com>.

Table 1. EVM-Compatible Device Data Sheets

Device	Literature Number	Device	Literature Number
ADS1278	SBAS367	OPA1632	SBOS286
ADS1274	SBAS367	SN74LVC2G157	SCES207
ADS1178	SBAS373	TPS73018	SBVS054
ADS1174	SBAS373	TPS65131	SLVS493
REF5025	SBOS410	PCA9535	SCPS129
OPA2350	SBOS099		

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I²C is a trademark of NXP Semiconductors, Inc.

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1 EVM Overview

The ADS1x7xEVM-PDK is an evaluation module kit that includes an EVM, MMB0 motherboard and software. As a stand-alone PCB, the ADS1x7xEVM is useful for prototyping designs and firmware. It can be connected to any modular EVM system interface card.

1.1 Features

ADS1x7xEVM Features:

- Contains all support circuitry needed for the ADS1178/ADS1278/ADS1174/ADS1274
- Voltage reference options: external or onboard
- Clock options: External clock source (PLL or DSP supplied) or 27MHz onboard crystal oscillator
- GPIO access
- Compatible with the TI Modular EVM System

ADS1x7xEVM-PDK includes the ADS1x7xEVM board with the DSP-based MMB0 motherboard, that can be used with ADCPro™ to quickly evaluate the device.

This manual covers the operation of the ADS1x7xEVM-PDK. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1178EVM/ADS1278EVM/ADS1174EVM/ADS1274EVM. For clarity of reading, this manual will refer only to the ADS1278EVM or ADS1x7xEVM-PDK, but operation of the EVM and kit for the ADS1178/ADS1274/ADS1174 is identical, unless otherwise noted.

2 Quick Start

This section provides a QuickStart guide to quickly begin evaluating the ADS1x7xEVM with ADCPro.

2.1 Default Jumper/Switch Configuration

Figure 1 shows the jumpers found on the EVM and the respective factory default conditions for each.

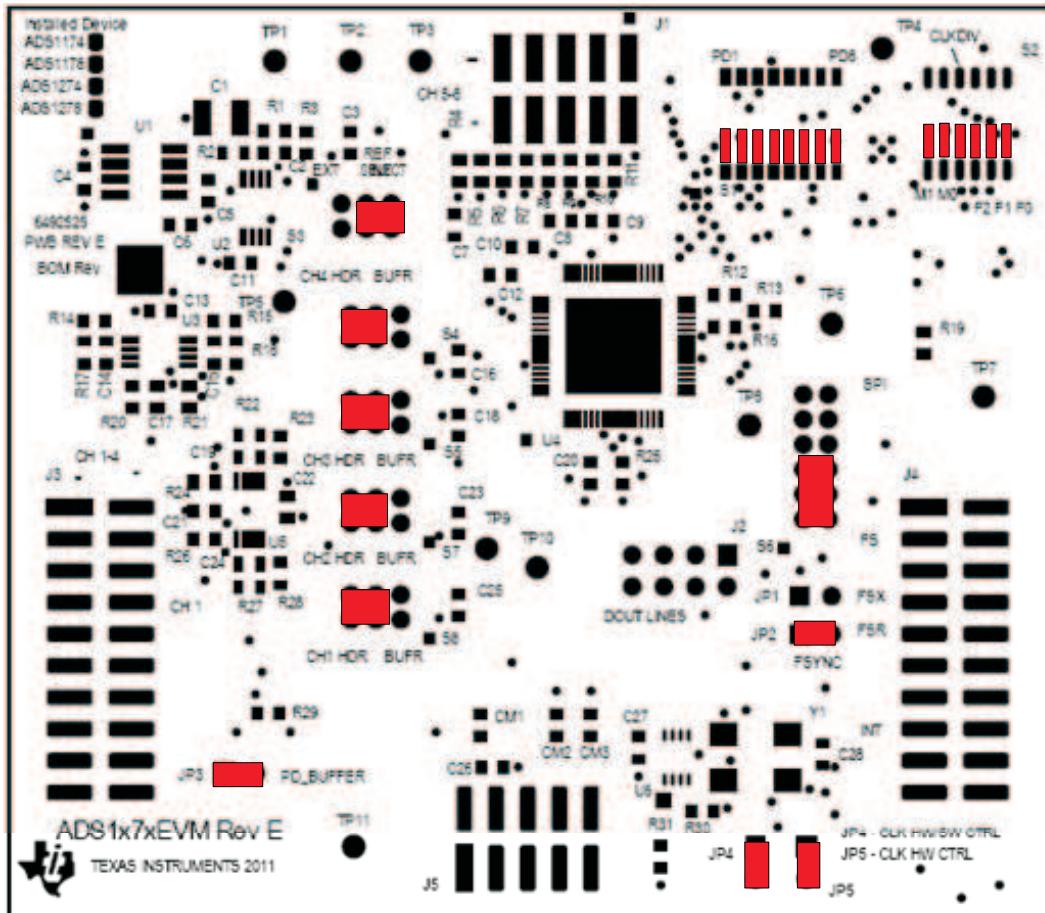


Figure 1. ADS1x7xEVM Default Jumper Locations

Table 2 lists the jumpers and switches and the factory default conditions.

Table 2. Default Jumper/Switch Configuration

Switch	Default Position	Switch Description
S1	All OFF (Down)	Powerdown channel DIP switches (Hardware control)
S2	All OFF (Down)	Mode, Format, and CLKDIV DIP switches(Hardware control)
S3	INT (Right)	On-board Voltage Reference Selected
S4	Header connected to converter (Left)	Channel 4 header connected to converter (not buffered)
S5	Header connected to converter (Left)	Channel 3 header connected to converter (not buffered)
S6	FS (Down)	FS serial interface format
S7	Header connected to converter (Left)	Channel 2 header connected to converter (not buffered)
S8	Header connected to converter (Left)	Channel 1 header connected to converter (not buffered)

Table 2. Default Jumper/Switch Configuration (continued)

Switch	Default Position	Switch Description
Jumper		
J1	Open	FSX NOT connected to SYNC/DRDY
J2	Short	FSR connected to SYNC/DRDY
J3	Short	Input buffer op-amps are powered down
J4	Short	Clock source selection using software control
J5	Short	External clock source selected (invalid since using software control)

2.2 *ADS1x7xEVM-PDK Kit Operation*

To prepare to evaluate the ADS1278 with the ADS1x7xEVM-PDK, complete the following steps:

1. Verify the jumpers on the ADS1x7xEVM are as shown in [Figure 1](#) (note that these settings are the factory-configured settings for the EVM).
2. Using [ADCPro HW/SW Installation Manual](#), verify the MMB0 jumpers are in the default position and install ADCPro and ADS1278EVM plug-in software. Complete hardware connection and driver installation as part of [ADCPro HW/SW Installation Manual](#) using the below settings.
 - MMB0 J13A → Open
 - MMB0 J13B → Short
 - No additional power connections are required
3. Plug the ADS1278EVM onto the MMB0 (if not already connected). The female portion of J3, J5 and J4 on the EVM align with male connectors J7, J4, and J5 respective on the MMB0.
4. Connect the included AC adapter to the MMB0.

CAUTION

Do not misalign the pins when plugging the ADS1278EVM into the MMB0. Check the pin alignment of J3, J5, and J4 carefully before applying power to the PDK.

3 Quick Reference

Table 3 provides a quick summary of the connections required for operation of the EVM as a stand-alone

Table 3. Critical Connections

Function		Header/Pin	Pin Name	Description
SPI	CS	N/A	N/A	N/A
	SCLK	J5.3	CLKX	SCLK
	DIN	J5.11	DX	Data In
	DOUT	J5.13	DR	Data Out
	Interrupt	J5.15	INT	FSYNC
Power	1.8V	J3.7	+1.8VD	Digital supply
	3.3V	J3.9	+3.3VD	Digital supply
	5.0V	J3.3	+5VA	Analog supply
Analog Inputs	Channels 1-4	J1.1-8		Analog Inputs
	Channels 5-8	J3.3-10		Analog Inputs (ADS1278 and ADSADS1178 only)

CAUTION

When using the EVM as part of the ADS1278EVM-PDK, the DIP switches S1 and S2 must all be switched so that they are down, toward the center of the board. Failure to do so may damage the EVM.

3.1 Analog Inputs

The analog inputs for the ADS1278EVM are connected to J1 and J3. Channels 1-4 connect to J1 and provisions are provided to buffer these signals before being connected to the converter. Switches S4-S5 and S7-S8 control whether the buffered or unbuffered signal is connected to the ADS1278. Channels 5-8 connect to J3 and have an RC filter available to filter the input before connecting to the converter. Channels 5-8 do not have provisions for buffering the signal.

3.2 Digital Control

The digital control signals can be applied directly to J4 (top or bottom side).

3.3 Power Supply

The ADS1278EVM requires power rails as follows:

- 5.0V analog supply - supplied by MMB0 motherboard via J13B
- 3.3V digital supply - supplied by MMB0 motherboard
- 1.8V digital supply - supplied by MMB0 motherboard

3.4 Voltage Reference

The ADS1278EVM has two options for the reference voltage. Switch S3 selects the reference voltage from either the buffered REF5025 or a external reference voltage that is connected to the reference pins of J3.

4 Using the ADS1178EVM-PDK/ADS1278EVM-PDK Plug-in ADCPro

The ADS1278EVM-PDK plug-in for ADCPro provides complete control over all settings of the ADS1278. It consists of a tabbed interface (see [Figure 2](#)), with different functions available on different tabs. The tabs are:

- Channel Enable
- Settings
- About

The user can adjust the ADS1178EVM/ADS1278EVM settings when not acquiring data. During acquisition, all controls are disabled and settings may not be changed. When a setting is changed on the ADS1178EVM/ADS1278EVM plug-in, the setting immediately updates on the board.

Settings on the ADS1178EVM/ADS1278EVM correspond to settings described in the [ADS1278 product data sheet](#) product data sheet.

4.1 Top Level Controls

You can adjust the ADS1278EVM settings when you are not acquiring data. During acquisition, all controls are disabled and settings may not be changed.

The effective data rate of the ADS1278 depends upon settings of the Clock Freq and Operating Mode. The **Data Rate** indicator in the upper right corner of the plug-in interface (see [Figure 2](#)) is always visible and updates whenever a setting changes that affects the data rate.

4.2 Channel Enable Tab

The ADS1278 can acquire data from one to eight channels simultaneously. The *Channel Enable* tab (as shown in [Figure 2](#)) provides the control to power on or off each channel.

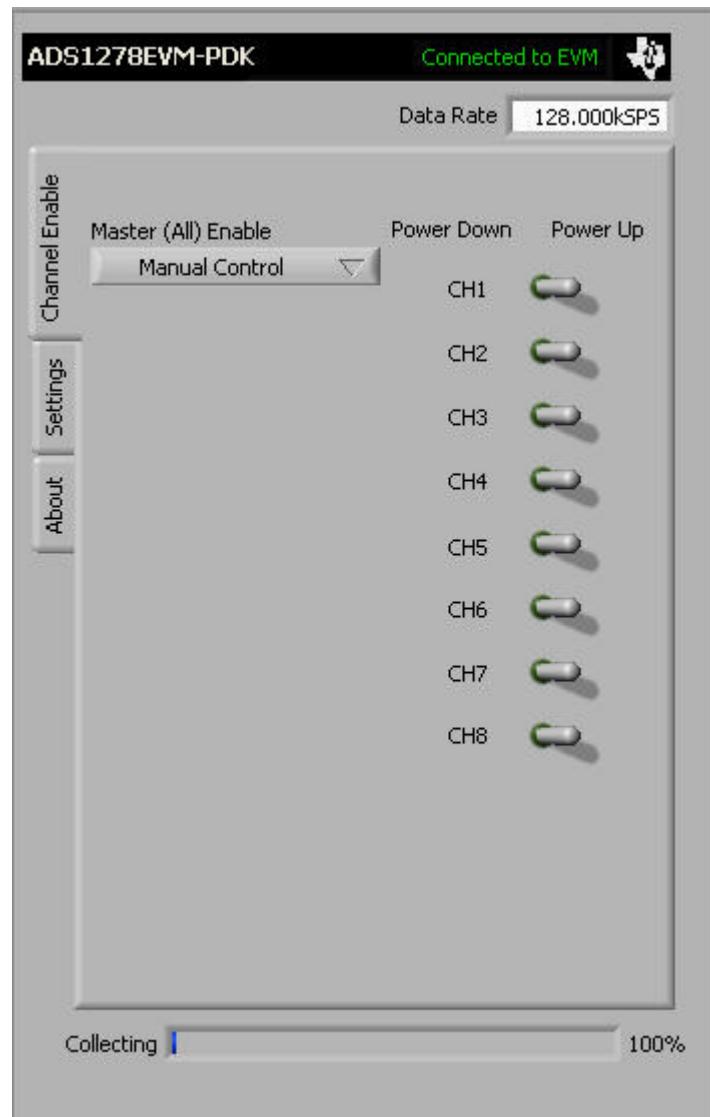


Figure 2. Channel Enable

The **Master (All) Enable** control allows for the selection of channels to convert. *Manual Control* allows channel enable control via **CH1** through **CH8** selector switches. *All Channels Enabled* and *All Channels Disabled* turn all the selector switches either ON or OFF.

4.3 **Settings Tab**

The **Settings** tab allows for the selection of the various clock frequencies, operating mode, data format, and other settings.

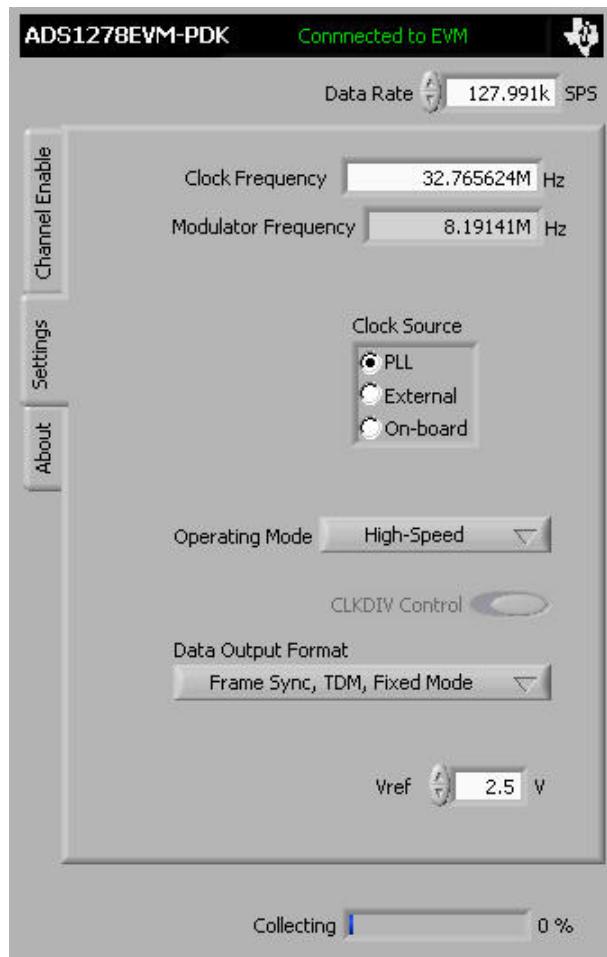


Figure 3. Clock Settings and Mode

The **Clock Source** control selects the input clock source for the ADS1278. The clock can be selected from the MMB0 *PLL*, an *External* source, or use the *On-board* oscillator.

The **Modulator Frequency** indicator shows the ADS1278 modulator frequency based on the clock source.

The **Clock Frequency** control allows the user to input the desired clock frequency when the *PLL* clock source is selected. Once the frequency is entered, the software finds the closest frequency for the PLL to synthesize (and which is within the maximum allowable frequency for the mode selected). This clock frequency is configured in the PLL and overwrites the user entered value in the **Clock Frequency** indicator.

The **Operating Mode** control allows selection of the converter operating mode: *High-Speed*, *High-Resolution*, *Low-Power*, or *Low-Speed*.

The **CLKDIV** control can be set to **0** or **1**.

The **Data Output Format** allows selection of the data output formats. For the ADS1278EVM software, the formats are limited to the *Frame Sync*, *TDM Format*. The available options select whether the software collects data for all channels *Fixed Mode* or only channels that are powered up *Dynamic Mode*.

The **Vref** control allows the user to input the current Vref value being used by the data converter. This control does not change the actual reference voltage, but is required for the software to process the data correctly for display.

The maximum clock frequency is shown for the different converter options in [Table 4](#).

Table 4. Operating Modes: Clock Frequency

Operating Mode	CLKDIV	Frequency (MHz)
High-Speed	1	32.768
High-Resolution	1	27
Low-Power	1	27
Low-Power	0	13.5
Low-Speed	1	27
Low-Speed	0	5.4

4.4 About Tab

The **About** tab provides information on the EVM hardware and software versions.

Plug-in Version is software version of ADCPro plug-in.

Firmware Version is firmware version loaded and running on the processor.

5 ADS1278EVM Hardware Details

The ADS1278EVM is designed to easily interface with multiple control platforms. Dual-row, header/socket combinations at J3, J4, and J5 allow connection to external circuitry for evaluation and debug.

5.1 Jumpers and Switches

Jumpers and Switches function shown in table below

Table 5. Jumper and Switch Descriptions

Jumper/Switch	Functions	Descriptions
J1	FSYNC/DRDY Source	Short to select FSR as the source ⁽¹⁾
J2	FSYNC/DRDY Source	Short to select FSX as the source ⁽¹⁾
J3	Analog Input Buffers Powerdown	Short - input buffers powered down Open - input buffers powered up
J4	Hardware/Software Control of Clock Source	Short - Software control Open - Hardware control
J5	Internal/External Clock Select (Hardware control)	Short - External clock source selected Open - Internal clock source selected
S1	GPIO2	Hardware control for GPIO2 (set to OFF position for use with software)
	GPIO3	Hardware control for GPIO3 (set to OFF position for use with software)
	GPIO4	Hardware control for GPIO4 (set to OFF position for use with software)
	CLKDIV	Hardware control for CLKDIV (set to OFF position for use with software)
	GPIO0	Hardware control for GPIO0 (set to OFF position for use with software)
	GPIO1	Hardware control for GPIO1 (set to OFF position for use with software)
S2	Powerdown Channel 1	Hardware control for PWDN1 (set to OFF position for use with software)
	Powerdown Channel 2	Hardware control for PWDN2 (set to OFF position for use with software)
	Powerdown Channel 3	Hardware control for PWDN3 (set to OFF position for use with software)
	Powerdown Channel 4	Hardware control for PWDN4 (set to OFF position for use with software)
	Powerdown Channel 5 ⁽²⁾	Hardware control for PWDN5 (set to OFF position for use with software)
	Powerdown Channel 6 ⁽²⁾	Hardware control for PWDN6 (set to OFF position for use with software)
	Powerdown Channel 7 ⁽²⁾	Hardware control for PWDN7 (set to OFF position for use with software)
	Powerdown Channel 8 ⁽²⁾	Hardware control for PWDN8 (set to OFF position for use with software)
S3	Converter Reference source selector	Selects source for reference - buffered on-board ref or header (external)
S4	Channel 4 Input source selector	Selects Channel 4 input source - header or input buffer Left - header Right - input buffer
S5	Channel 3 Input source selector	Selects Channel 3 input source - header or input buffer Left - header Right - input buffer

⁽¹⁾ Only one of FSYNC/DRDY signals should be connected at a time (J1 or J2).

⁽²⁾ Channels 4-8 only available for ADS1278 and ADS1178.

Table 5. Jumper and Switch Descriptions (continued)

Jumper/Switch	Functions	Descriptions
S6	Serial Interface format	FS - Frame Sync format ⁽³⁾ SPI - SPI-compatible mode ⁽³⁾
S7	Channel 2 Input source selector	Selects Channel 2 input source - header or input buffer Left - header Right - input buffer
S8	Channel 1 Input source selector	Selects Channel 1 input source - header or input buffer Left - header Right - input buffer

⁽³⁾ Refer to [Section 5.5.1](#) for more details.

5.2 Power-Down, Mode, and Format Control

The ADS1278 has several pins to control the power-down of individual channels, and select the mode and format for the digital interface.

For users of the ADS1278EVM as a stand-alone module, these pins may be pulled high or low through DIP switches S1 and S2 (see [Table 5](#)). Refer to the [ADS1278 product data sheet](#) for complete details on these pins and which state sets which options.

For use in the ADS1x7xEVM-PDK, the state of these pins is controlled by software, using the I²C port expander on the EVM. When using the EVM with the EVM-PDK, the DIP switches S1 and S2 must all be switched down (toward the center of the board). The ADS1278EVM-PDK software checks at startup to verify that these switches are set correctly, and generates an error message for incorrect settings. The software cannot detect if the switches are changed after startup.

CAUTION

When using the ADS1x7xEVM-PDK, the DIP switches S1 and S2 must all be switched down (toward the center of the board). Failure to do so may damage the EVM.

5.3 Clock Source

The ADS1278 clock can come from one of several sources: the onboard 27MHz crystal oscillator, a clock supplied by a processor on the TOUT pin (J4.17), or an external clock source connected between J4.17 (TOUT) and J4.18 (DGND).

If the onboard 27MHz oscillator is selected, the device can be run in high-speed mode, high-resolution mode, low-power mode, or low-speed modes with CLKDIV set to 1.

If the performance of the device must be explored with CLKDIV set to 0 in the low-power and low-speed modes, an external clock must be provided to the board, either using the TOUT connection or having an external clock source connected to J18. The same condition is true if frequencies other than the 27MHz provided by the onboard oscillator must be investigated.

5.4 Analog Headers, J1 and J3

For maximum flexibility, the ADS1278EVM is designed for easy interfacing to multiple analog sources. These headers/socket provide access to the analog input pins of the ADS1278.

Four of the analog input sources (Channels 1–4) connect directly to J3 (top or bottom side) or through signal-conditioning modules available for the modular EVM system. These inputs have provisions to buffer the inputs using THS4521 before connecting to the converter. Switches S4-5 and S7-8 provide the capability to connect either the header directly or through a buffer. When the buffers are not selected, the op-amps used for buffering can be powered down by shorting JP3.

Analog input sources (Channels 5-8) are connected directly to J1. These inputs can be filtered by installing passive components in the option filter circuitry. By default, the resistors are populated with 0Ω resistors and the capacitors are not installed. No circuitry is provided to buffer these signals before connecting to the converter.

Table 6. J3: Primary Analog Interface Pinout

Description	Signal	Pin Number		Signal	Description
Analog Input Channel 4 Negative	ANN4	J3.1 ⁽¹⁾	J3.2	ANP4	Analog Input Channel 4 Positive
Analog Input Channel 3 Negative	ANN3	J3.3	J3.4	ANP3	Analog Input Channel 3 Positive
Analog Input Channel 2 Negative	ANN2	J3.5	J3.6	ANP2	Analog Input Channel 2 Positive
Analog Input Channel 1 Negative	ANN1	J3.7	J3.8	ANP1	Analog Input Channel 1 Positive
Analog Ground	AGND	J3.9	J3.10	Not Connected	Not used for this design
Analog Ground	AGND	J3.11	J3.12	Analog Ground	AGND
Analog Ground	AGND	J3.13	J3.14	Not Connected	Not used for this design
Not used for this design	Not Connected	J3.15	J3.16	Not Connected	Not used for this design
Analog Ground	AGND	J3.17	J3.18	EXTREFN	External Reference negative input
Analog Ground	AGND	J3.19	J3.20	EXTREFP	External Reference positive input

⁽¹⁾ Pin 1 is top left-hand corner, located next to reference designator.

Table 7. J1: Secondary Analog Interface Pinout

Description	Signal	Pin Number		Signal	Description
Not used for this design	Not Connected	J3.1 ⁽¹⁾	J3.2	Not Connected	Not used for this design
Analog Input Channel 8 Negative	ANN8	J3.3	J3.4	ANP8	Analog Input Channel 8 Positive
Analog Input Channel 7 Negative	ANN7	J3.5	J3.6	ANP7	Analog Input Channel 7 Positive
Analog Input Channel 6 Negative	ANN6	J3.7	J3.8	ANP6	Analog Input Channel 6 Positive
Analog Input Channel 5 Negative	ANN5	J3.9	J3.10	ANP5	Analog Input Channel 5 Positive

⁽¹⁾ Pin 1 is top right-hand corner, located next to reference designator.

5.5 Digital Interface

The digital signals are controlled via DSP interface or I²C ICs on the EVM. Some of the digital control pins allow control via hardware or software methods. See [Section 5.2](#) for details on these pins and their operation. The digital control signals can be applied directly to the EVM or by connecting the EVM to a DSP or micro controller interface board, such as the MMB0 if purchased as part of the ADS1278EVM-PDK, the [5-6K Interface](#) or [HPA-MCUInterface](#) boards which are available from Texas Instruments. For a list of compatible interface and/or accessory boards for the EVM or the ADS1278, see the relevant product folder on the TI web site.

5.5.1 Digital Format Control

The ADS1278 allows the serial interface to be used in two different formats: an SPI-compatible mode and a frame-sync format. Switch S6 switches between these two formats:

- **SPI** format configures the signals as follows:

- The SCLK input of the converter is driven by the serial port signal CLKX, pin J5.3.
- The signal from the selected source for the clock (see [Section 5.3, Clock Source](#)) is connected to the CLKR pin (J5.5) allowing the serial port of a processor to be synchronized to the converter's master clock.
- The signal from the selected clock source is routed to the CLK input of the converter.
- Port P10 of the I²C port expander U18 is connected to a logic high level, so that the position of switch S12 can be read back by software.
- **FS** format configures the signals as follows:
 - The SCLK input of the converter is driven by the serial port signal CLKR, pin J5.5.
 - The signal from the selected clock source is connected to the CLKX pin (J5.3), allowing the serial port of a processor to be synchronized to the converter's master clock.
 - The CLK input of the converter is driven by the CLKR signal (J5.5). This ensures that the CLK and SCLK signals have the same phase and the correct ratio as outlined in the data sheet of the device.
 - Port P10 of the I²C port expander U18 is connected to a logic low level, so that the position of switch S12 can be read back by software.

For use in the ADS1278EVM-PDK, S6 must be in the **FS** position, which is the factory default setting.

Switching to **SPI** format will allow users to connect the EVM to any SPI-compatible processor not supporting the frame-sync mode. If this format is selected, keep in mind that the high-speed mode will not operate at full speed (32.768MHz) because of the limitations outlined in the device product data sheet.

5.5.2 Serial Data Interface, J5

This header/socket provides access to the digital control and serial data pins of the ADC.

All logic levels on J5 are 3.3V CMOS, except for the I²C™ pins. These pins conform to 3.3V I²C rules. [Table 8](#) describes the J5 serial interface pins.

Table 8. J5, Serial Interface Header

	Signal Name	Pin Number (J4)		Signal Name	Function
Synchronize channels input	SYNC	1 ⁽¹⁾	2	MODE0	Select bit 0 of converter MODE
SPI clock	SCLK	3	4	DGND	Digital ground
SCLK clock	CLKR	5	6	MODE1	Select bit 1 of converter MODE
DRDY/FSYNC source 1	DRDY/FSYNC	7	8	FORMAT0	Select bit 0 of FORMAT to select Frame-Sync/SPI Protocol
DRDY/FSYNC source 2	DRDY/FSYNC	9	10	DGND	Digital ground
ADS1278 SPI data in	DIN	11	12	FORMAT1	Select bit 1 of FORMAT to select Frame-Sync/SPI Protocol
ADS1278 data out	DOUT1 ⁽²⁾	13	14	FORMAT2	Select bit 2 of FORMAT to select Frame-Sync/SPI Protocol
DRDY/FSYNC to DSP (interrupt)	DRDY/FSYNC	15	16	SCL	I ² C clock
Can be used to provide a clock from a processor	CLK	17	18	DGND	Digital ground
Clock source select (SW mode)	CLK Select	19	20	SDA	I ² C data

⁽¹⁾ Pin 1 is top left-hand corner, located next to reference designator.

⁽²⁾ DOUT1 buffered through a D flip-flop. See [Section 5.5.3.1](#) below.

Some pins on J5 have weak pull-up/down resistors. These resistors provide default settings for many of the control pins. Many pins on J5 correspond directly to ADS1278 pins. See the [ADS1278 product data sheet](#) for complete details on these pins.

5.5.3 Data Output Signals

5.5.3.1 *DOUT on Digital Interface J5*

In TDM mode, the data from all eight channels can be observed on the DOUT1 pin of the converter. The DOUT1 signal is used by the ADS1x7xEVM-PDK to read back and display all the channels. The digital data output pin on the digital interface header J5 is connected to DOUT1 signal via a D flip-flop. The D flip-flop provides a half cycle delay in order to align the data correctly to reach the higher speeds of the device. Otherwise, the propagation delay from the MSB in Frame Sync mode may result in missing the MSB out of the data word.

5.5.3.2 *DOUTx Header, J2*

All the data output signals (DOUT1 to DOUT8) can be monitored on J2. [Table 9](#) illustrates the pinout for J2.

Table 9. J2, DOUTx Header

Data Out Line	Pin Number		Data Out Line
DOUT1	1 ⁽¹⁾	2	DOUT2
DOUT3	3	4	DOUT4
DOUT5	5	6	DOUT6
DOUT7	7	8	DOUT8

⁽¹⁾ Pin 1 is top right-hand corner, located next to reference designator.

5.6 Power Supply Header, J3

J3 is the power-supply input connector. [Table 10](#) lists the configuration details for J3. Supplies of 1.8V, 3.3V, and 5.0V are required for operation of the EVM. When using the EVM as part of the EVM-PDK, these voltages are generated by the MMB0 and no external supplies are required. For operation as a stand-alone EVM, the power supplies should be connected as shown below.

Table 10. J3 Configuration: Power-Supply Input

Function	Pin Name	Pin Number (J5)		Pin Name	Function
Not used for this design	Not used	1 ⁽¹⁾	2	Not used	Not used for this design
+5V analog supply	+5VA	3	4	Not used	Not used for this design
Digital ground	DGND	5	6	AGND	Analog ground input
1.8V digital supply	+1.8VD	7	8	Not used	Not used for this design
3.3V digital supply	+3.3VD	9	10	N/A	Do not use

⁽¹⁾ Pin 1 is bottom left-hand corner, located next to reference designator.

NOTE: For monitoring the current from each supply, CM1, CM2, and CM3 (0Ω resistors) can be removed and replaced with sense resistors or ammeters.

The ADS1278 digital supplies are connected as follows:

- IOVDD supply is connected to the +1.8VD pin of the J3 header.
- DVDD supply is connected to the +3.3VD pin of the J3 header.

The ADS1278 analog supply, AVDD, is connected to the +5VA pin of the J3 header.

6 Schematic and Bill of Materials

A complete schematic for the ADS1x7xEVM is appended to this user's guide. The bill of materials is provided in [Table 11](#). Gerber files are available on request. Please e-mail support@ti.com or [E2E Community Forums](#) and ask for details on how to receive the files.

6.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the <http://www.ti.com>.)

Table 11. ADS1x7xEVM Bill of Materials

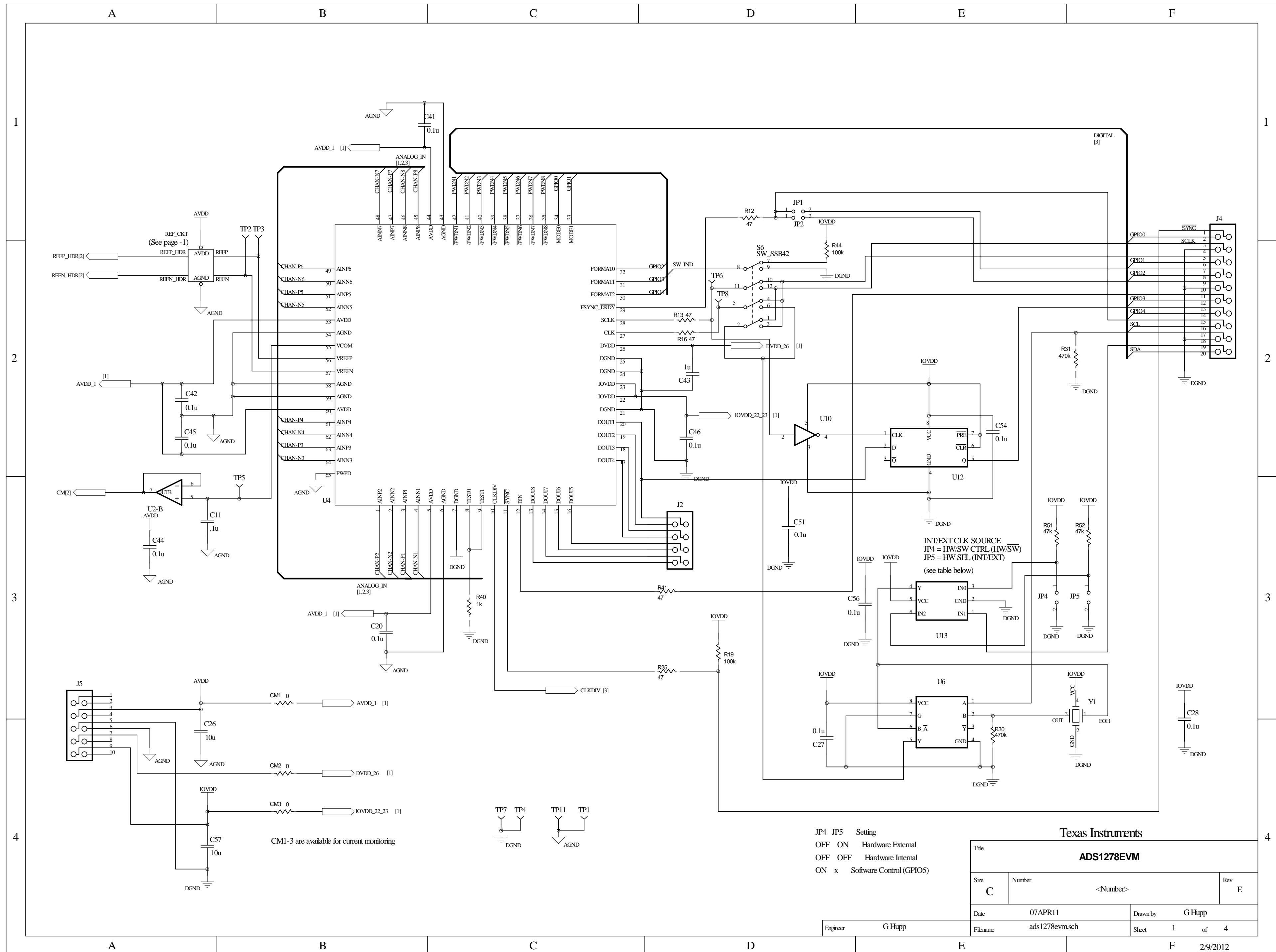
Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
1	1	100u	C1	Capacitor, Ceramic, X5R, 10V	Taiyo Yuden	LMK325BJ107MM-T
2	1	150n	C2	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E154K
3	25	0.1u	C3, C11, C13, C17, C20, C21, C22, C27, C28, C29, C38, C39, C40, C41, C42, C44, C45, C46, C49, C50, C51, C54, C55, C56, C58	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E104K
4	3	1.0u	C4, C6, C43	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E105K
5	4	10u	C5 C7 C26 C57	Capacitor, Ceramic, X5R, 10V	TDK	C1608X5R1A106M
6	4 ⁽¹⁾	2.2n	C8-10 C12	Capacitor, Ceramic, C0G, 50V	TDK	C1608COG1H222/*J
			C16 C18 C23 C25			
7	8	1.5n	C14-15 C19 C24 C47-48 C52-53	Capacitor, Ceramic, X7R, 25V	TDK	C1608X7R1E152M
			C30-37			
8	3	0	CM1-3	Resistor, Chip, 1/4W	Vishay Dale	CRCW06030000Z0EAHP
9	1 ⁽¹⁾		J1 (Top)	Header, SMT Vert. 5x2 pin, 100mil spacing	Samtec	TSM-105-01-T-DV-P
10	1		J5 (Top)	Header, SMT Vert. 5x2 pin, 100mil spacing	Samtec	TSM-105-01-T-DV-P
11	1		J5 (Bottom)	Header, SMT Vert. 5x2 pin, 100mil spacing	Samtec	SSW-105-22-F-D-VS-K
12	1		J2	Header, SMT Vert. 4x2 pin, 100mil spacing	Samtec	TSW-104-07-L-S
13	2		J3 J4	Header, SMT Vert. 10x2 pin, 100mil spacing	Samtec	TSM-110-01-T-DV-P
14	2		J3 J4 (Bottom)	Header, SMT Vert. 10x2 pin, 100mil spacing	Samtec	SSW-110-22-F-D-VS-K
15	5		JP1-JP5	Header, Male 2-pin, 100mil spacing	Samtec	TSW-102-07-L-S
16	1	2k	R1	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ202
17	18	1k	R2 R17-18 R20-22 R24 R26-27 R38-40 R42-43 R45-48	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ102
18	6	47	R3 R12-13 R16 R25 R41	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ470
19	8 ⁽¹⁾	0	R4-11	Resistor, Chip, 1/10W	Rohm	MCR03EZPJ000
20	8	49.9	R14-15 R23 R28 R36-37 R49-50	Resistor, Chip, 1/10W, 1%	Rohm	MCR03EZPJ49R9
21	3	100k	R19 R29 R44	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ104
22	2	470k	R30-31	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ474
23	2	100k	R32-33	Resistor Pack, 8x	Panasonic	EXB-2HV104JV
24	1	10k	R34	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ103
25	1	4.3k	R35	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ432
26	2	47k	R51-52	Resistor, Chip, 1/10W, 5%	Rohm	MCR03EZPJ473

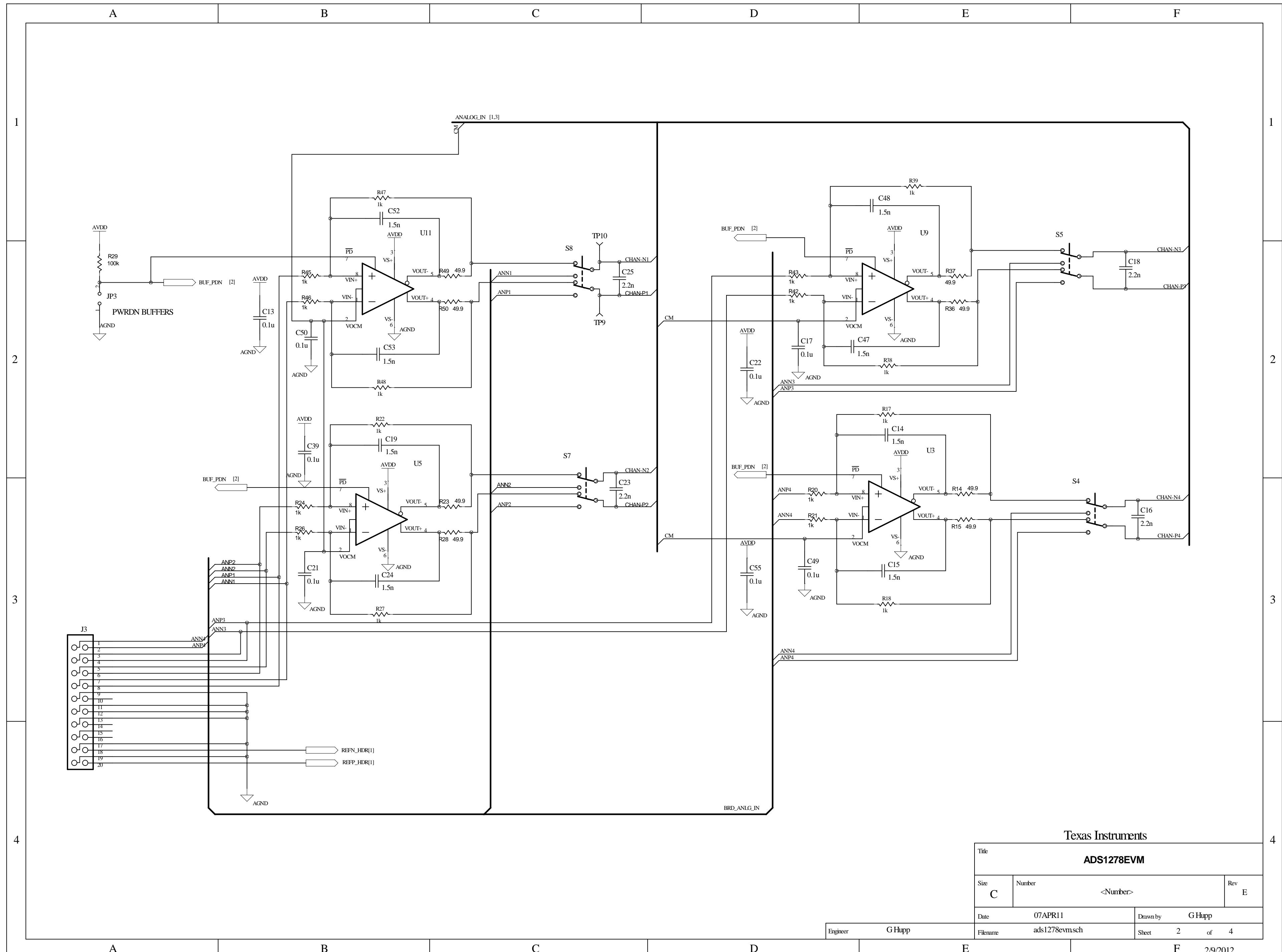
⁽¹⁾ These parts are not installed for ADS1274 and ADS1174

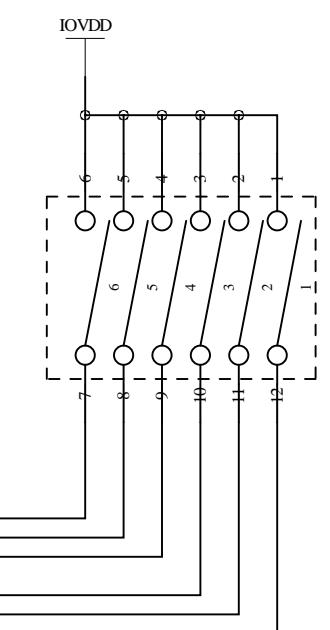
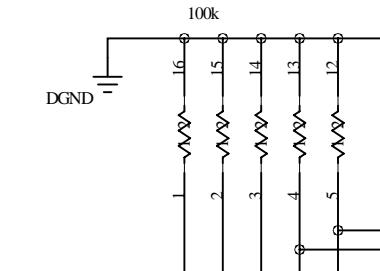
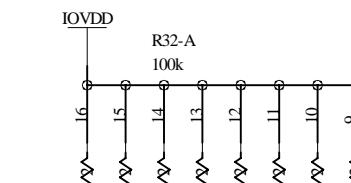
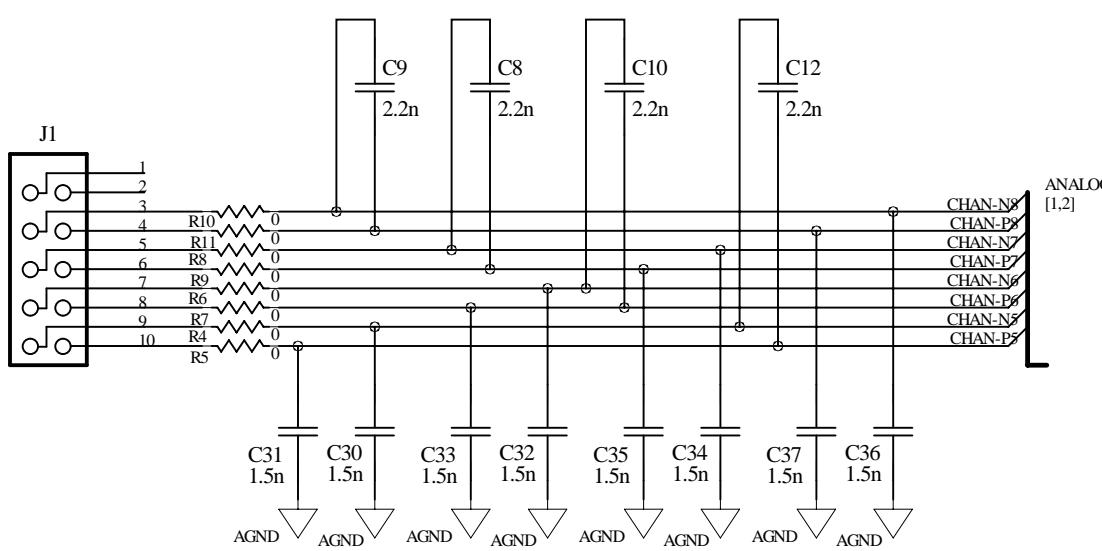
Table 11. ADS1x7xEVM Bill of Materials (continued)

Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
27	1		S1	Switch, SMD Low Profile 08 Position	CTS	218-8LPST
28	1		S2	Switch, 6 POS, SPST, Low Profile, SMT, 0.50 centers	CTS	218-8LPST
29	5		S3-5 S7-8	Switch, Slide DPDT, Low Profile	TE Connectivity	SSB22
30	1		S6	Switch, Slide, 4 x SPDT, SMD	TE Connectivity	SSB42
31	4		TP1 TP4 TP7 TP11	Test Point, Black, Thru Hole Color Keyed	Keystone	5001
32	2		TP6 TP8	Test Point, White, Thru Hole Color Keyed	Keystone	5002
33	5		TP2 TP3 TP5 TP9 TP10	Test Point, Red, Thru Hole Color Keyed	Keystone	5000
34	1		U1	IC, Precision Voltage Reference, 2.5V	TI	REF5025AID
35	1		U2	IC, Op Amp, High-Speed, Single-Supply, R-R	TI	OPA2350DGK
36	4		U3 U5 U9 U11	IC, Negative R-R Input, R-R Output, Fully Differential Amplifier	TI	THS4521DGK
37	1 ⁽²⁾		U4	IC, Quad/Octal, Simultaneous Sampling, 24-Bit A-D Converter	TI	ADS1278PAP
38	1		U6	Single 2 line To 1Line Data Selector/Multiplexer	TI	SN74LVC2G157DCT
39	1		U10	IC, Single Inverter	TI	SN74LVC1G04DBV
40	1		U12	IC, single Positive-Edge-Triggered D-Type Flip-Flop With Clear And Reset	TI	SN74LVC2G74DCU
41	1		U13	IC, Configurable Multiple-Function Gate	TI	SN74LVC1G97DCK
42	1		U14	IC, 256K CMOS Serial EEPROM	Microchip	24AA256-I/ST
43	2		U7-8	IC, Low Voltage 16-BIT I2C and SMBus Low-Power I/O Expander With Interrupt Output and Configuration Registers	TI	TCA9535RTW
44	1		Y1	Clock Oscillator, 27MHz	CTS	CB3LV-3I-27M0000
45	1			PCB, 3.31 In x 2.88 In x 0.062 In	Any	6492525
46	4			Shunt, 100-mil, Black	3M	929950-00

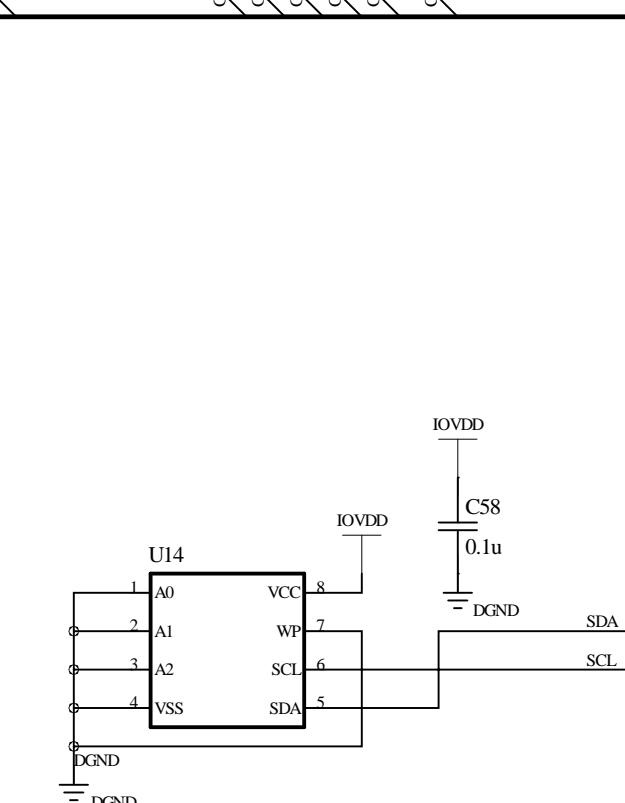
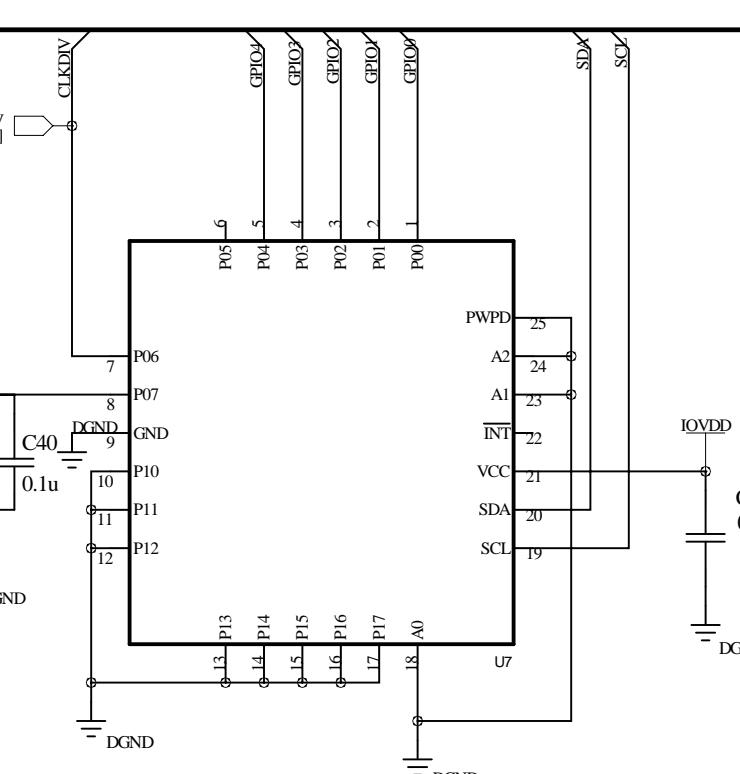
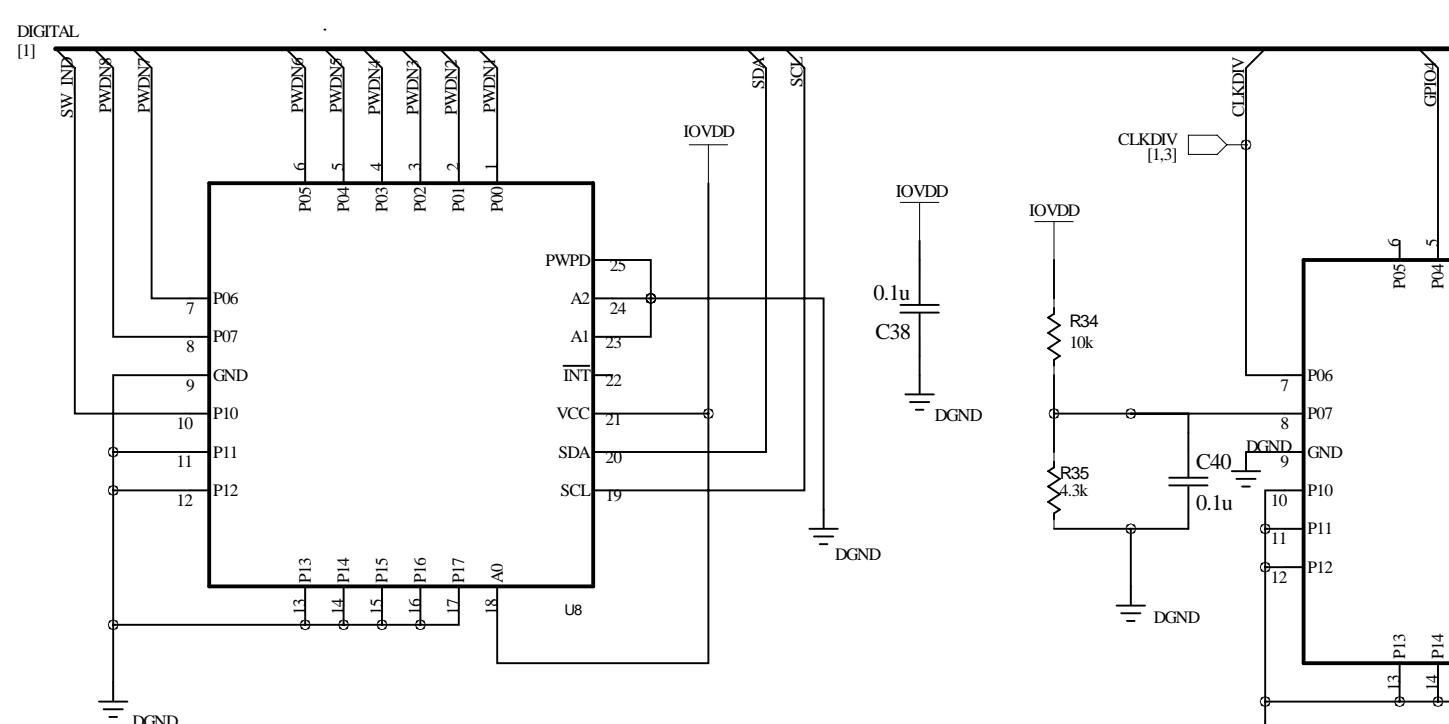
⁽²⁾ Installed for ADS1278EVM-PDK. For other EVM-PDKs, the appropriate device will be installed.







GPIO/Logic Connections



Texas Instruments

ADS1278EVM

Texas Instruments

ADS1278EVM		
Size	Number	Rev
C	<Number>	E
Date	07APR11	Drawn by G Hupp
Filename	ads1278evm.sch	Sheet 3 of 4

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/ kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this is strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

REGULATORY COMPLIANCE INFORMATION (continued)

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjukku-ku, Tokyo, Japan

<http://www.tij.co.jp>

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日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル
<http://www.tij.co.jp>

EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

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The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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